

Alpine/Snowboard 1.5

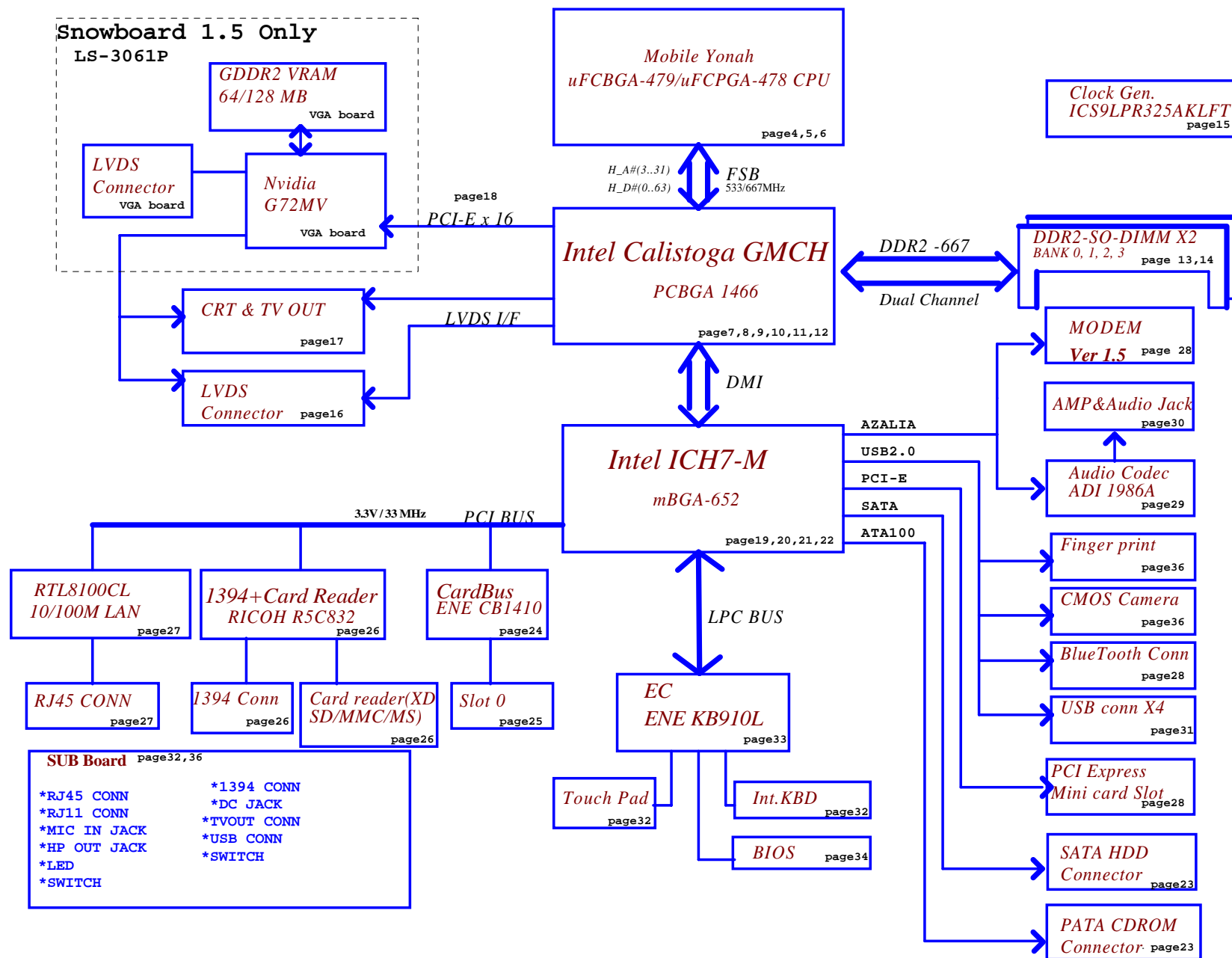
Schematics Document

Mobile Yonah uFCPGA with Intel
Calistoga_GM/PM+ICH7-M core logic

星期二, 二月 21, 2006

REV:0.1

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Voltage Rails

power plane	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V	+5VS
				+3VS +2.5VS +1.8VS +1.5VS +1.2VS +VGA_CORE +0.9VS +CPU_CORE +VCCP
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

O MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394	AD22	0	PIRQG/H
LAN	AD17	3	PIRQF
CardBus	AD20	2	PIRQA

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		

EC SM Bus2 address

ICH6 SM Bus address

Device	Address
Clock Generator (ICS954226)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
* 3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SKU ID	HDL00 SKU
* 0	UMA W/FPR W/BT
1	UMA WO/FPR W/BT
2	UMA W/FPR WO/BT
3	UMA WO/FPR WO/BT
4	VGA W/FPR W/BT
5	VGA WO/FPR W/BT
6	VGA W/FPR WO/BT
7	VGA WO/FPR WO/BT

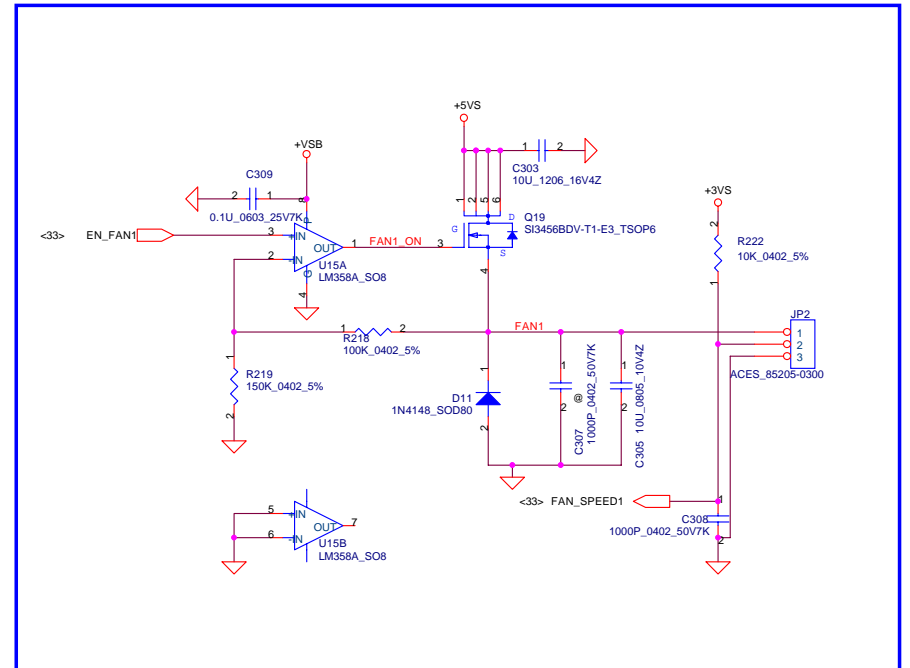
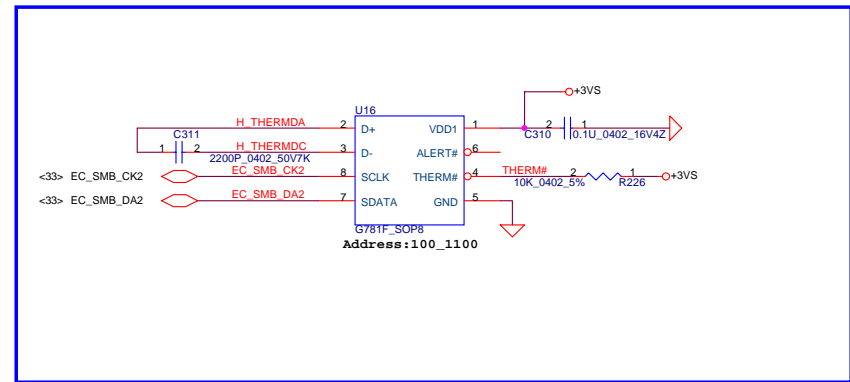
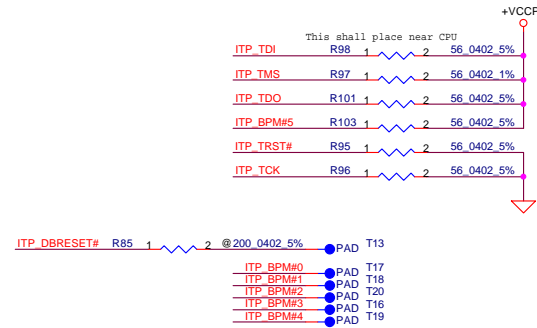
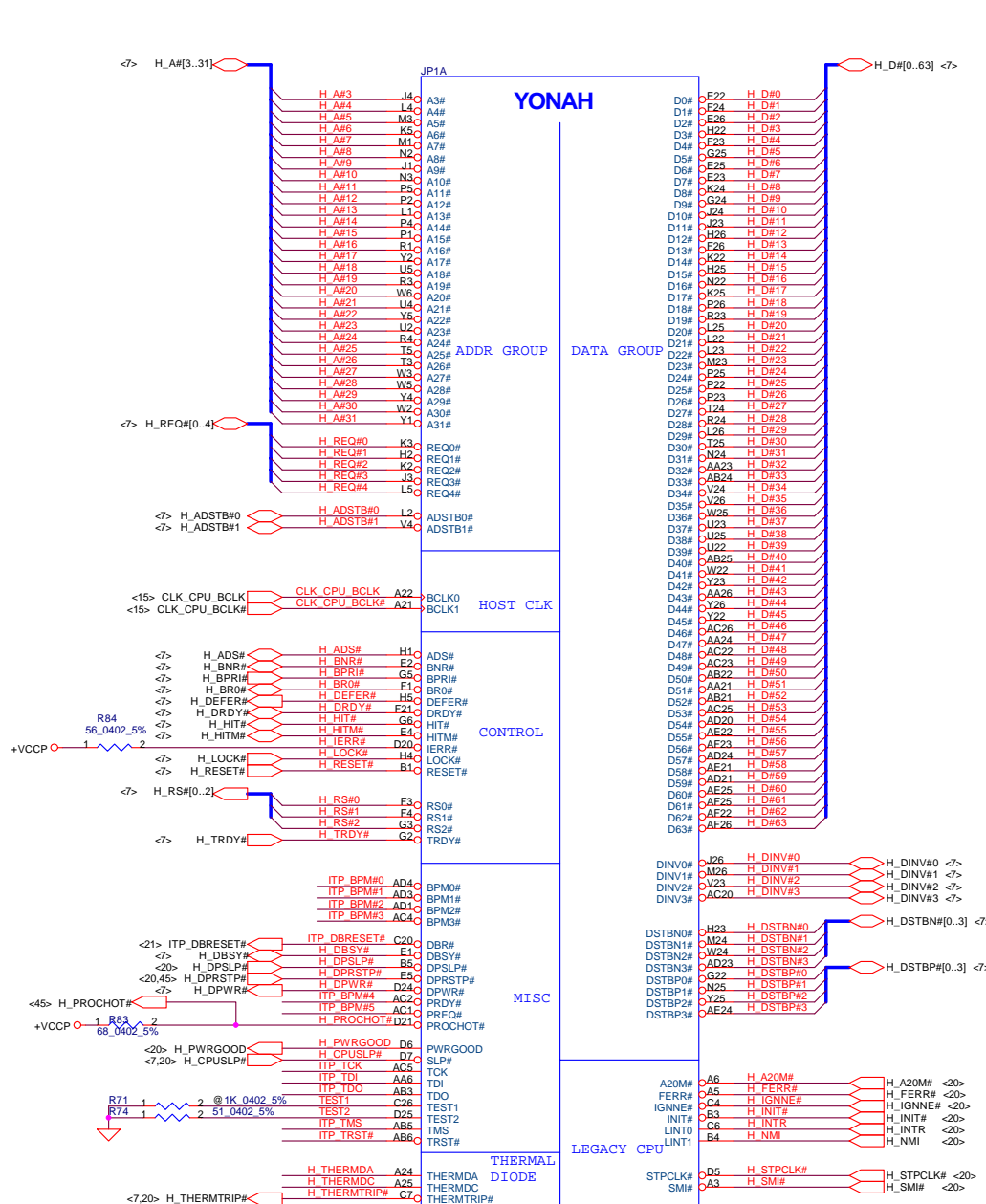
MB ID	HDL00 SKU
H	HDL00
L	HDL10

BOM Structure

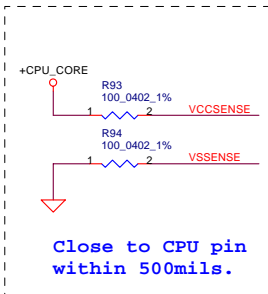
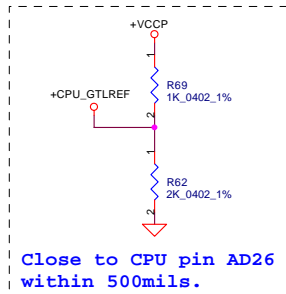
MARK	FUNCTION
@	NC FOR ALL
GIGA@	8110SBL(SCL)Giga LAN
10/100@	8100CL 10/100Mb LAN
UMA@	Internal 945GM
VGA@	External G7xM

USB PORT LIST

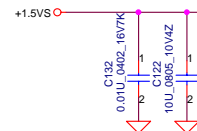
PORT	DEVICE
0	LEFT SIDE
1	BLUE TOOTH
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	FINGER PRINTER
6	RIGHT SIDE
7	NC



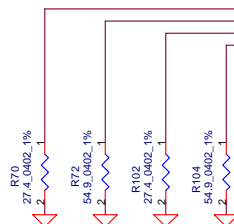
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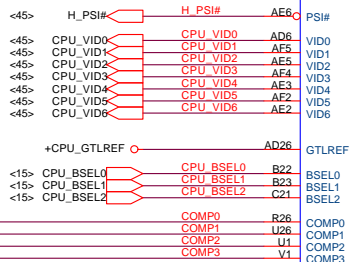
Length match within 25 mils
The trace width 18 mils space
7 mils



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

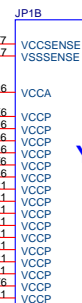


Resistor placed within
0.5" of CPU pin. Trace
should be at least 25
mils away from any
other toggling signal.



YONAH

POWER, GROUND, RESERVED SIGNALS AND NC

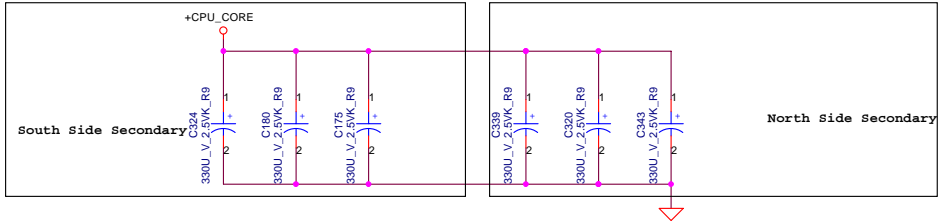
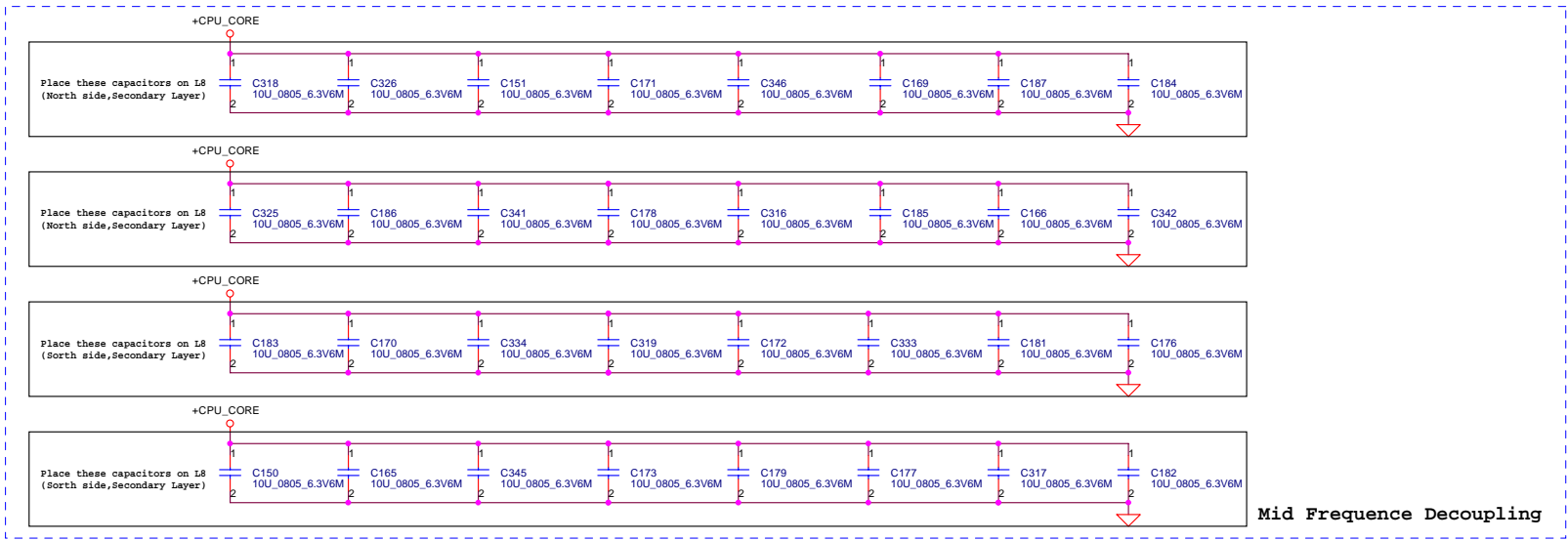


YONAH

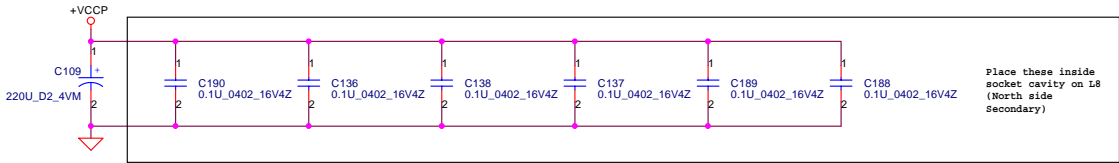
POWER, GROUND

TYCO_1-1674770-2_Yonah-D
ME@

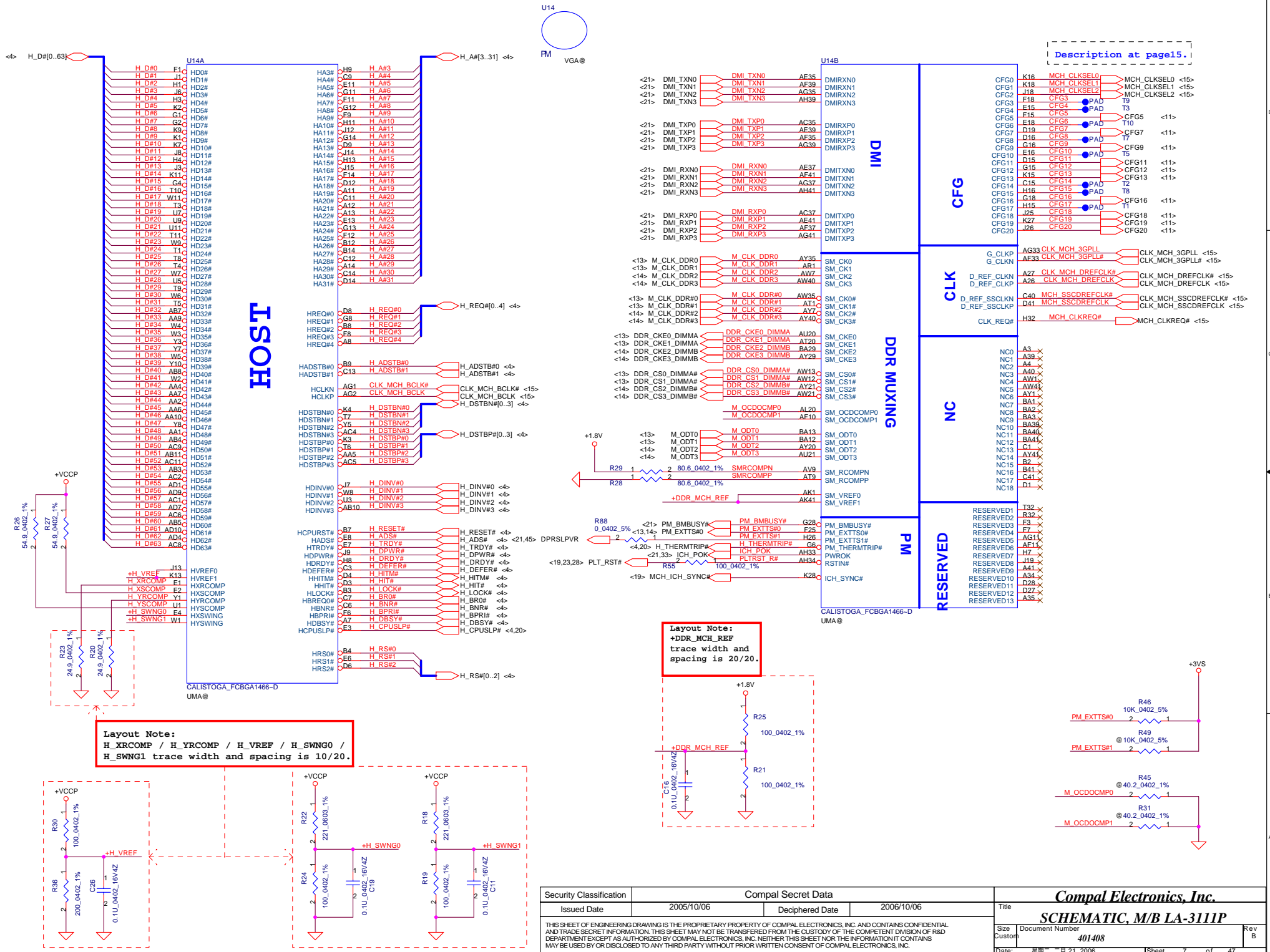
TYCO_1-1674770-2_Yonah-D
ME@



ESR <= 1.5m ohm
Capacitor > 1980uF



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Description at page15.

HOST

DMI

CFG

CLK

DDR MUXING

NC

PM

RESERVED

Layout Note:
+DDR_MCH_REF
trace width and
spacing is 20/20.

Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 /
H_SWNG1 trace width and spacing is 10/20.

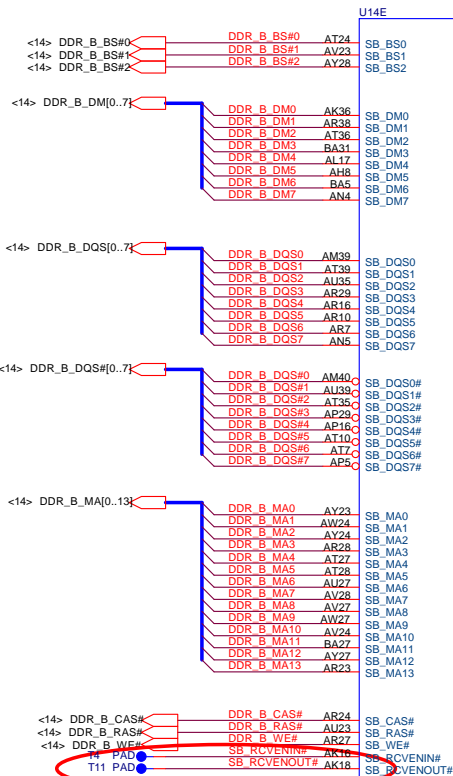
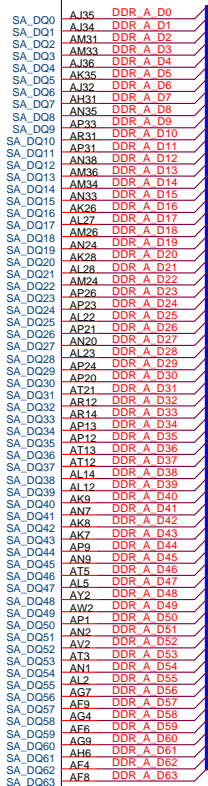
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check layout

U14D
CALISTOGA_FCBGA1466-D
UMA@

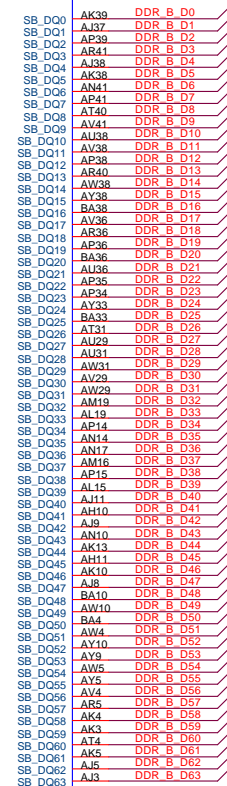
DDR SYS MEMORY A



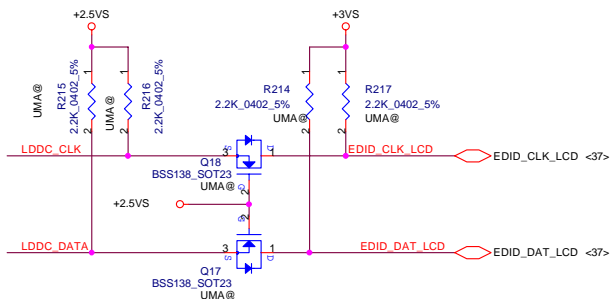
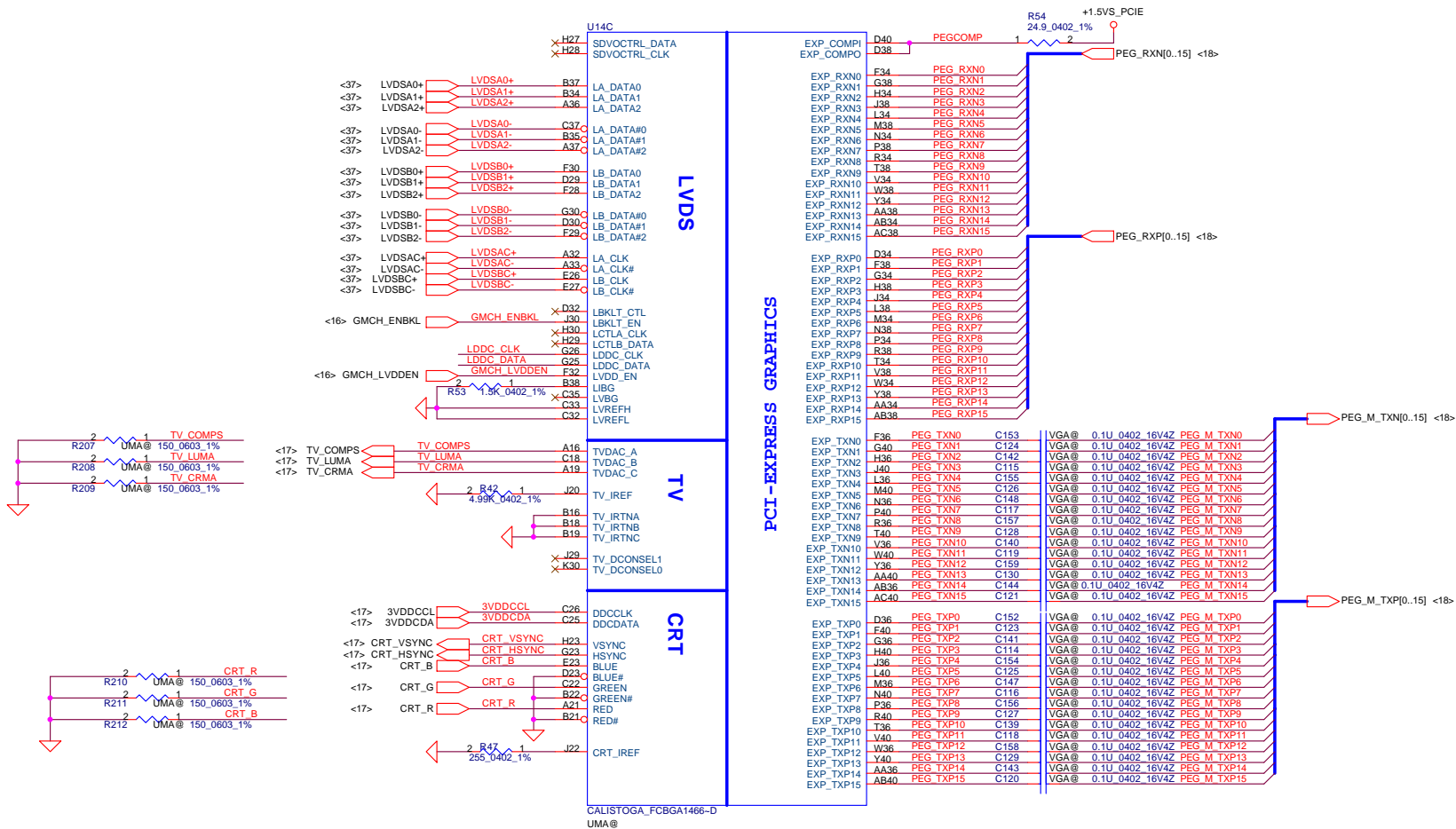
check layout

U14E
CALISTOGA_FCBGA1466-D
UMA@

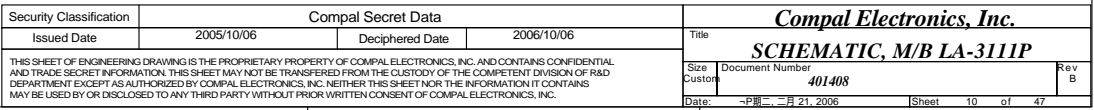
DDR SYS MEMORY B



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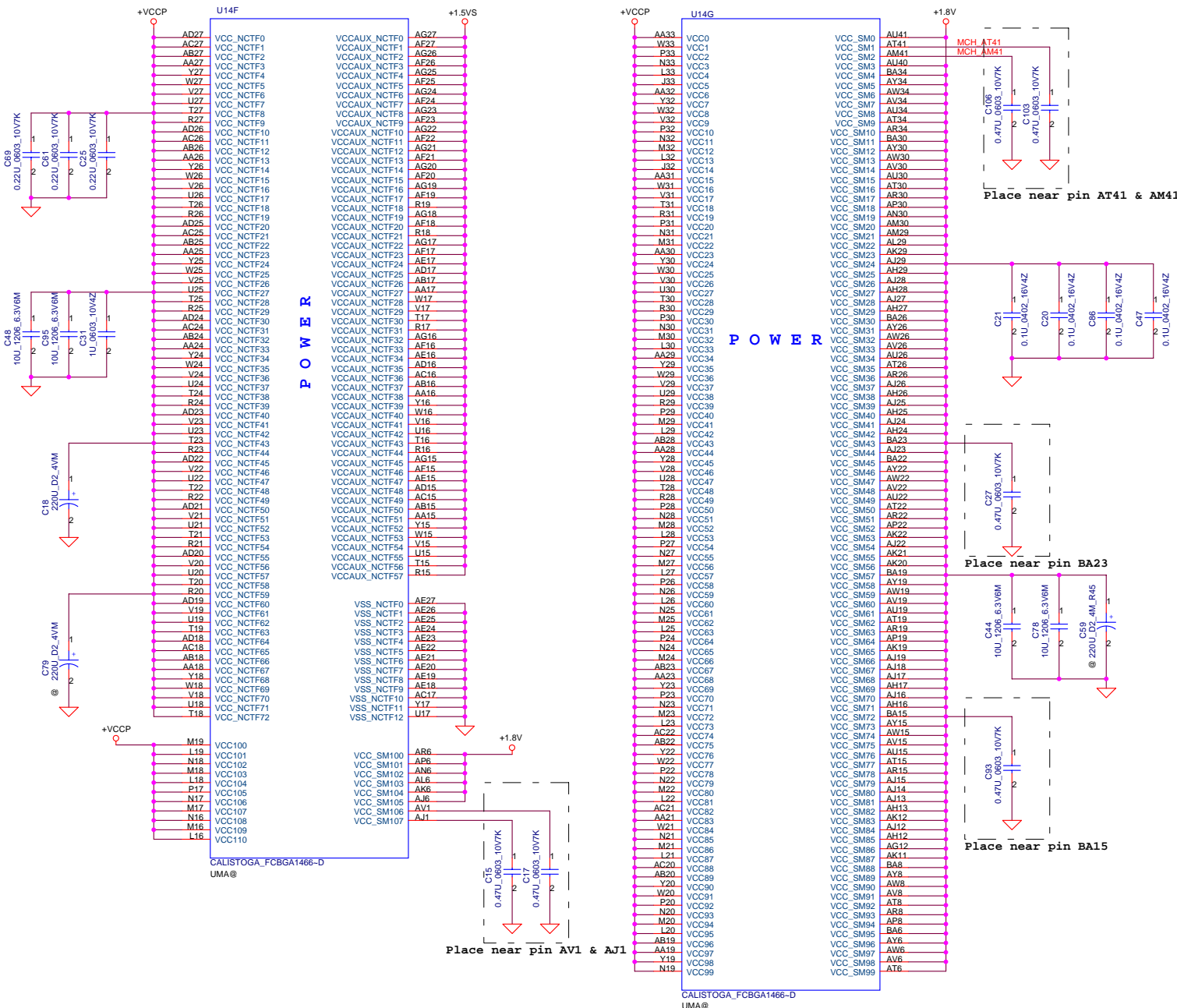
Strap Pin Table

CFG[3:17] have internal pull up

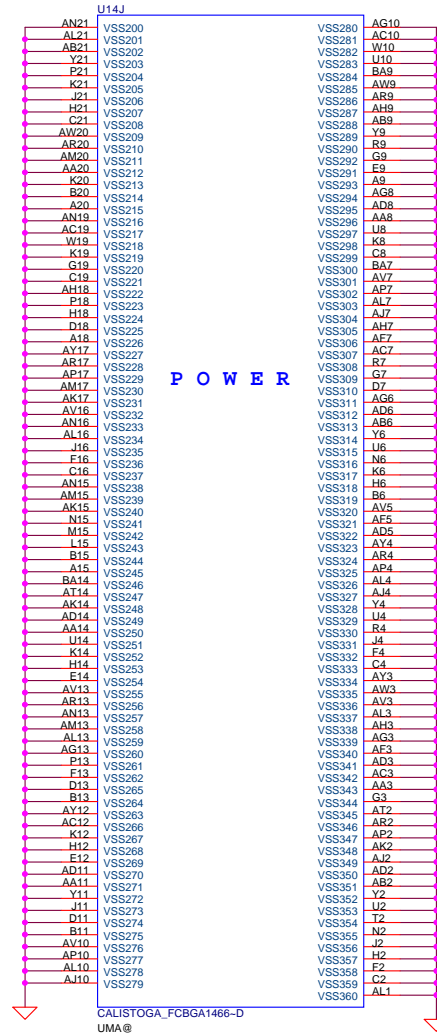
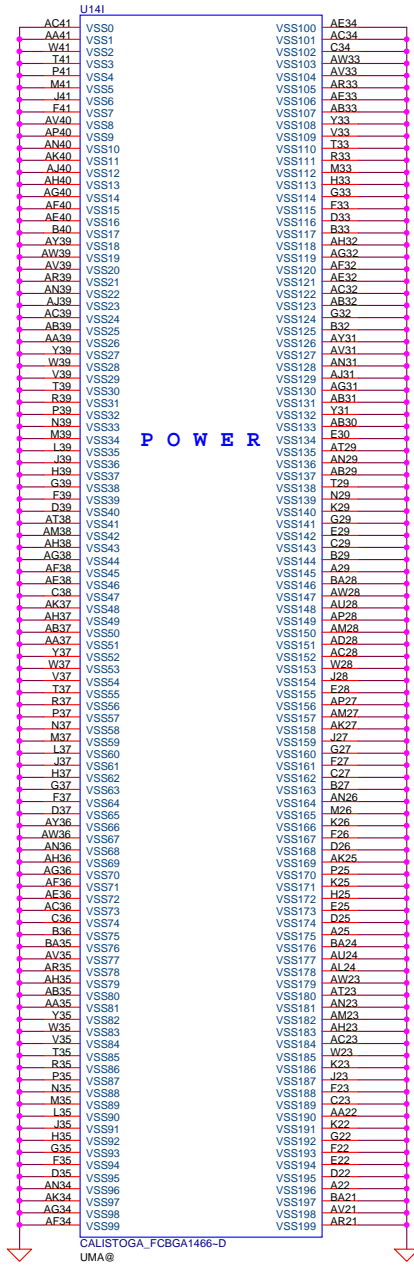
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4*(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation*(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled*(Default)
CFG10 CFG18	10 = 1.05V*(Default) 01 = 1.5V
CFG19	0 = Normal Operation*(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present*(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

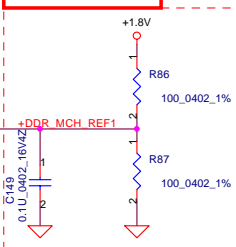
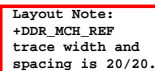
<7>	CFG5	R32	1	2	@ 2.2K 0402 5%
<7>	CFG7	R40	1	2	@ 2.2K 0402 5%
<7>	CFG9	R37	1	2	@ 2.2K 0402 5%
<7>	CFG11	R35	1	2	@ 2.2K 0402 5%
<7>	CFG12	R34	1	2	@ 2.2K 0402 5%
<7>	CFG13	R38	1	2	@ 2.2K 0402 5%
<7>	CFG16	R33	1	2	@ 2.2K 0402 5%
<7>	CFG18	R48	1	2	@ 1K 0402 5%
<7>	CFG19	R50	1	2	@ 1K 0402 5%
<7>	CFG20	R51	1	2	@ 1K 0402 5%



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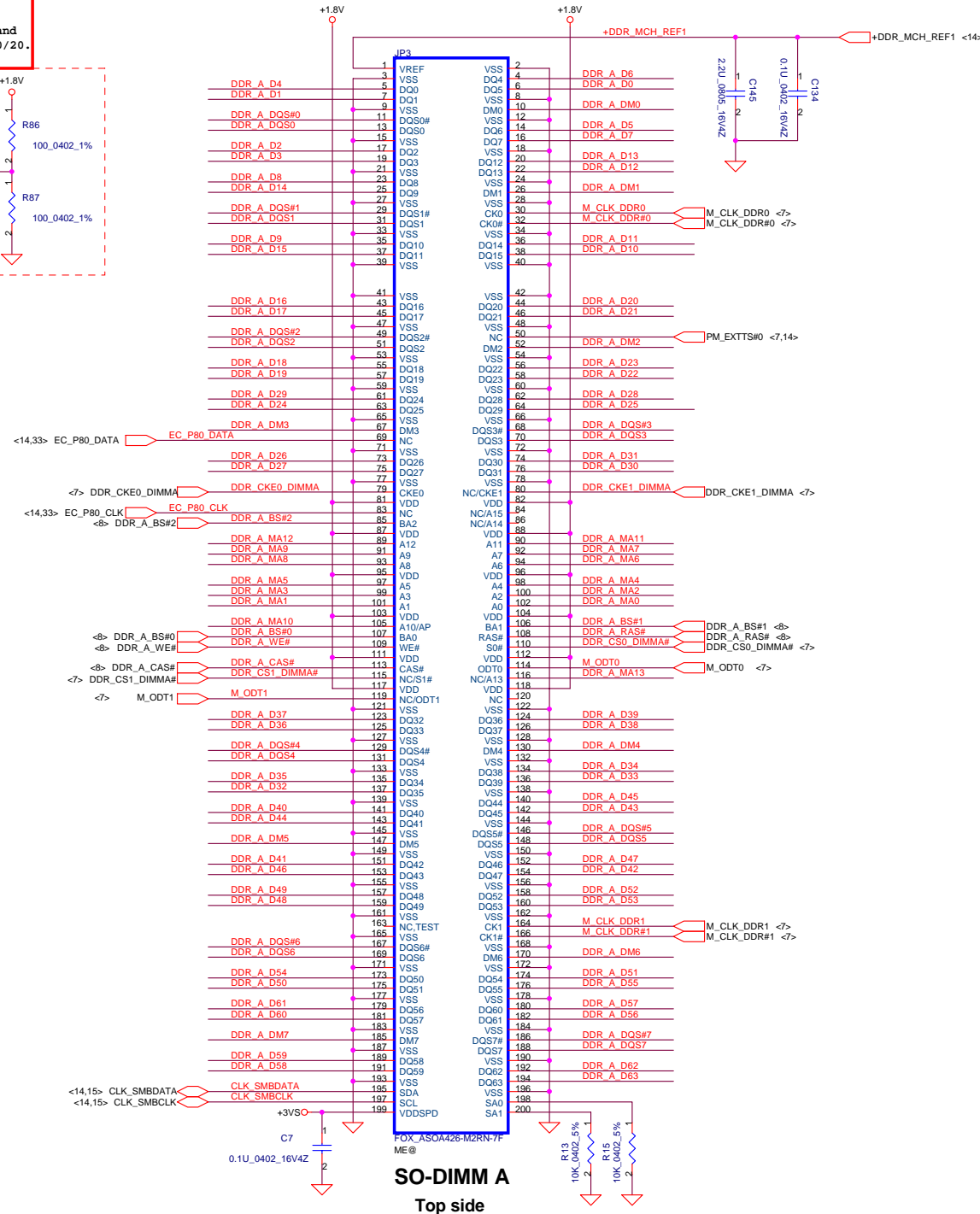


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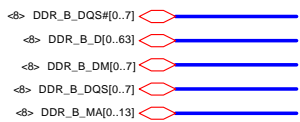
The schematic shows a horizontal power rail connected to a +1.8V source on the left. A series of decoupling capacitors, labeled C83 through C89, are connected in parallel to this rail. Each capacitor is represented by two parallel horizontal lines. The values for the capacitors are: C83 (0.1u, 0.047, 16V42), C84 (0.1u, 0.047, 16V42), C85 (0.1u, 0.047, 16V42), C86 (0.1u, 0.047, 16V42), C87 (0.1u, 0.047, 16V42), C88 (2.2u, 0.065, 16V42), and C89 (2.2u, 0.065, 16V42). The rail terminates on the right with a red triangle symbol pointing downwards, indicating a connection to ground.

Layout Note:
Place these resistor
closely JP41,all
trace length Max=1.5"

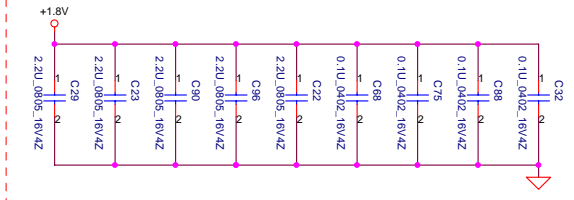


SO-DIMM A
Top side

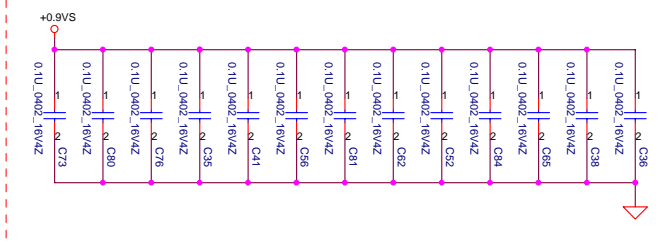
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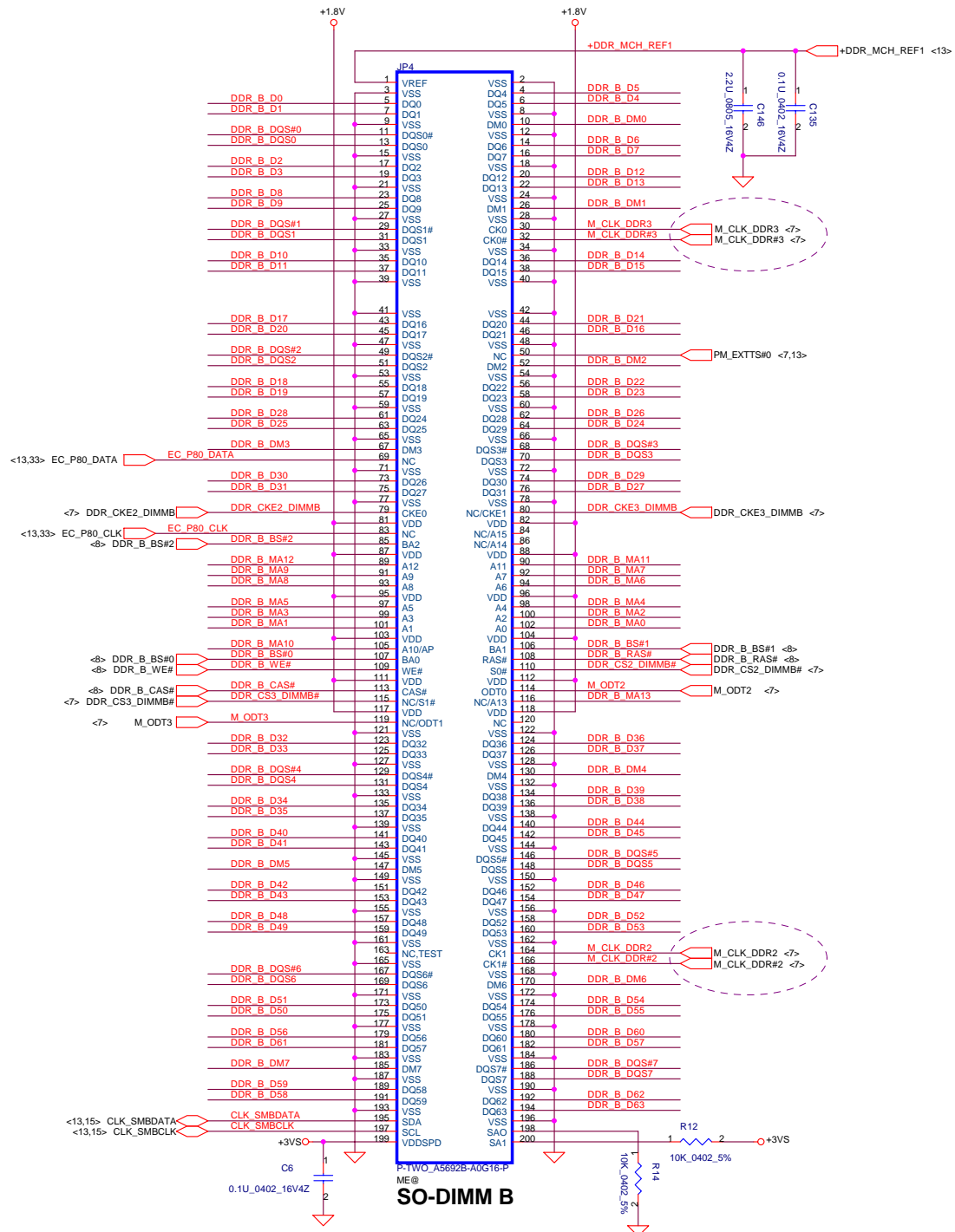
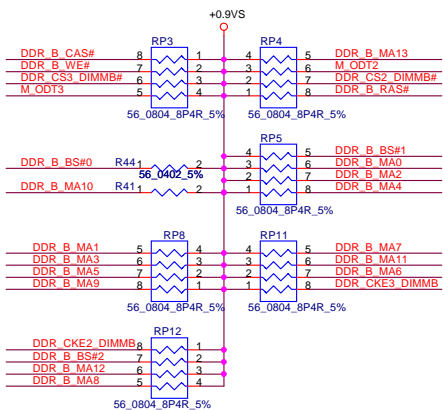
Layout Note:
Place near JP42



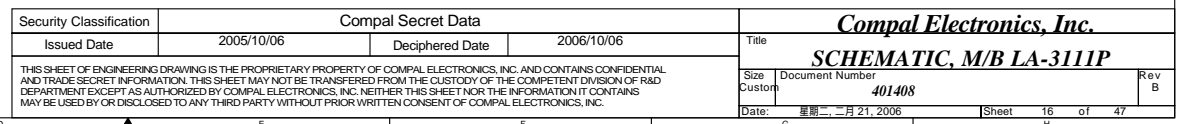
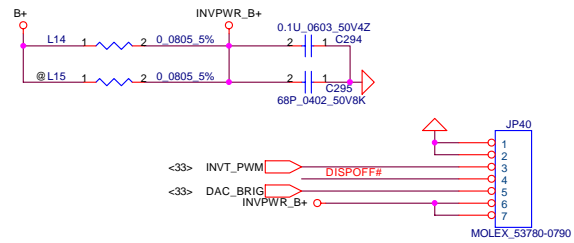
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



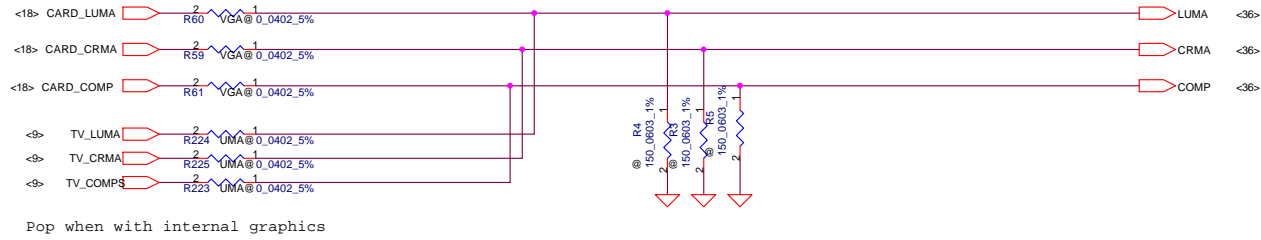
Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"



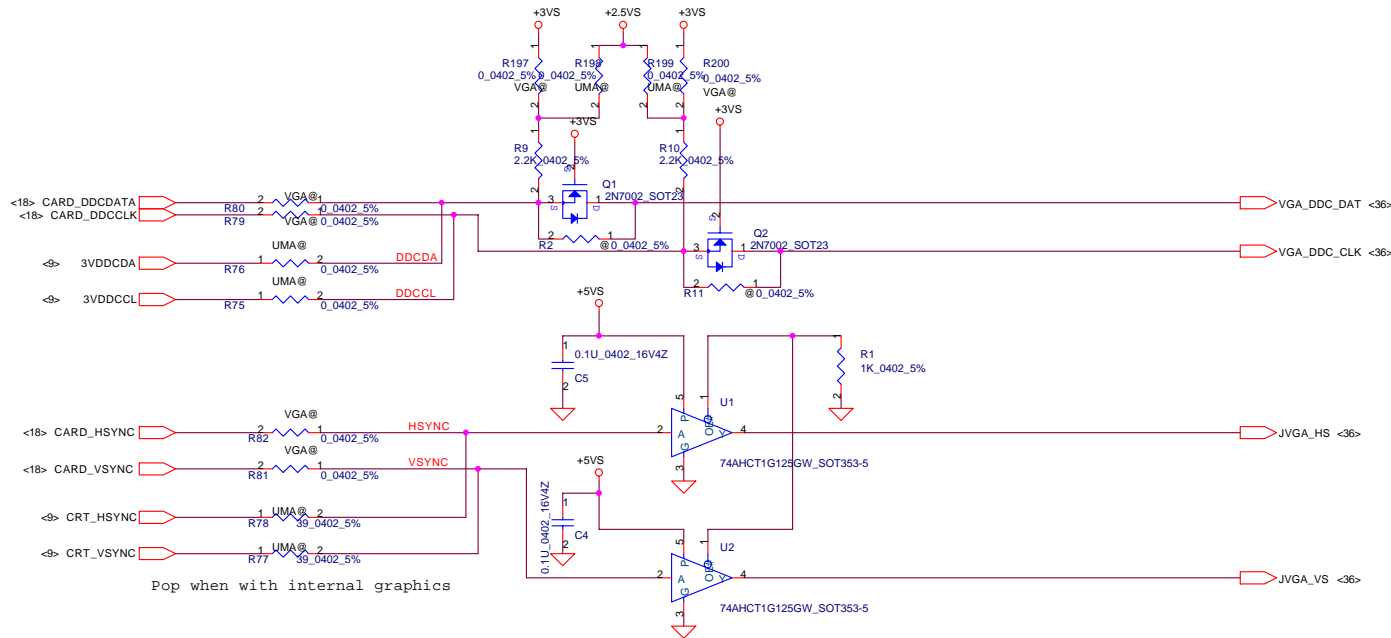
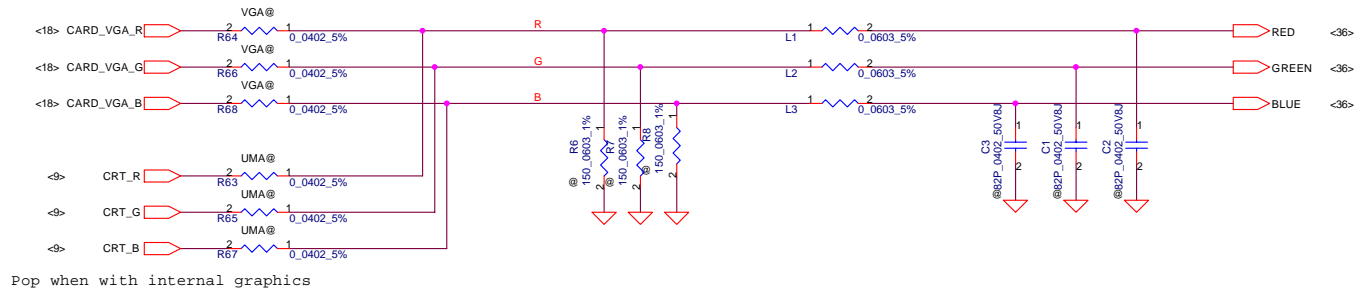
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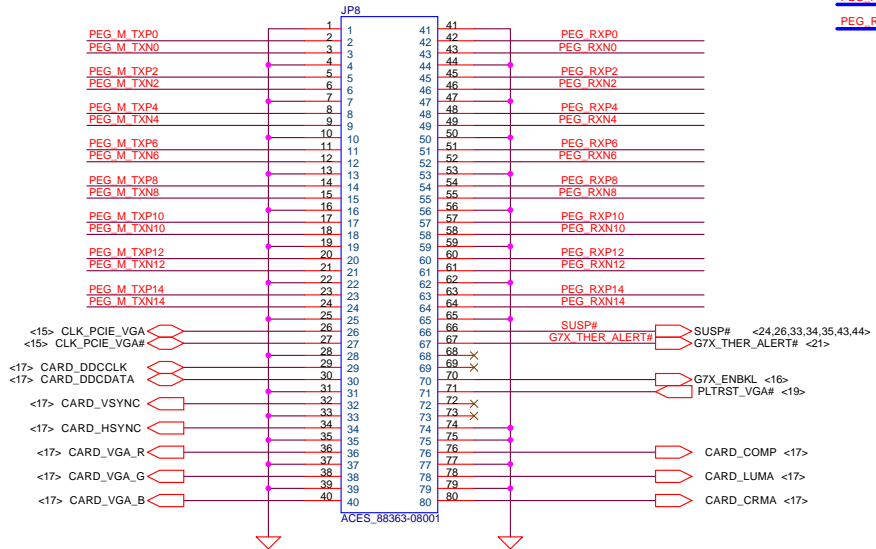
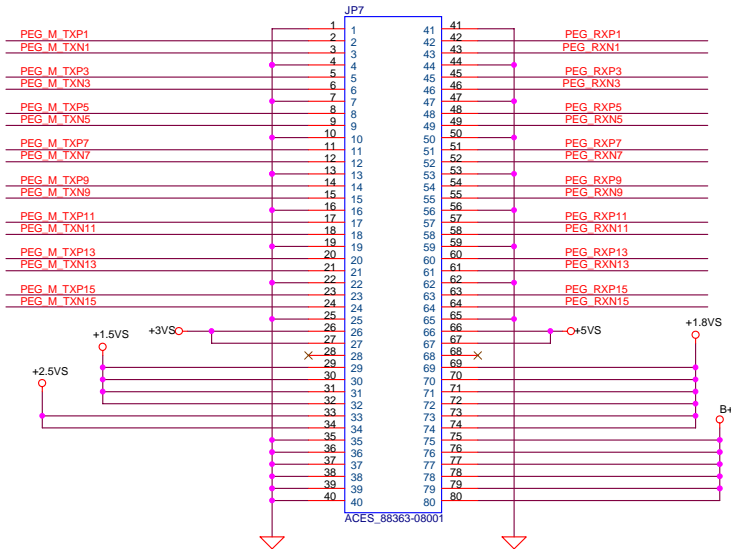
TV-OUT Conn.



CRT Conn.

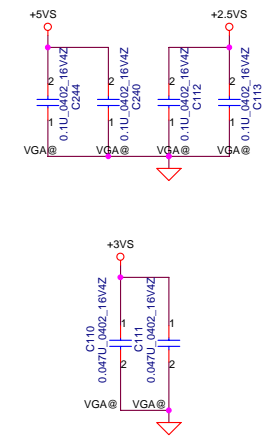


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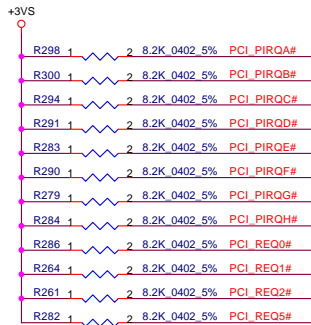
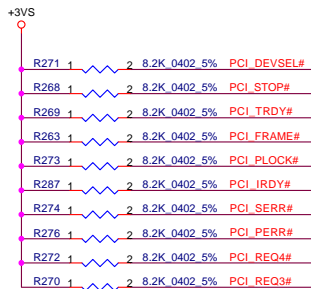
MAX. 4.06A @ 1.8V
MAX. 130mA @ 2.5V
MAX. 655mA @ 3.3V

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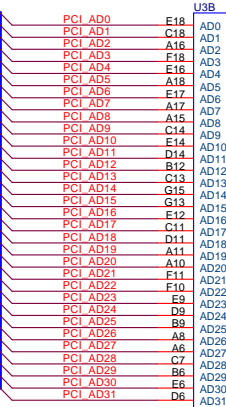


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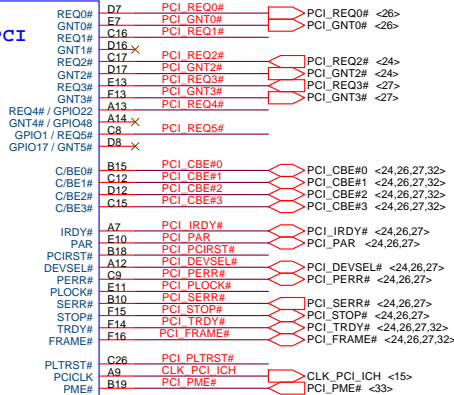
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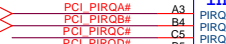


PCI



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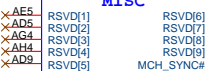
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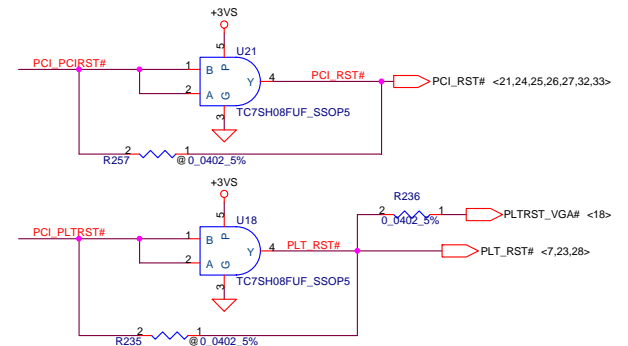
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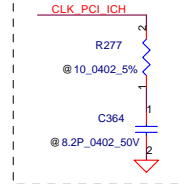
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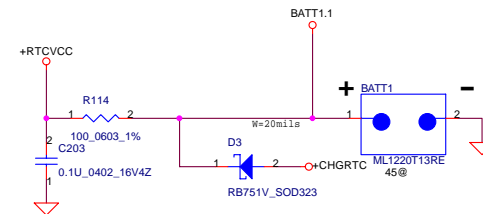
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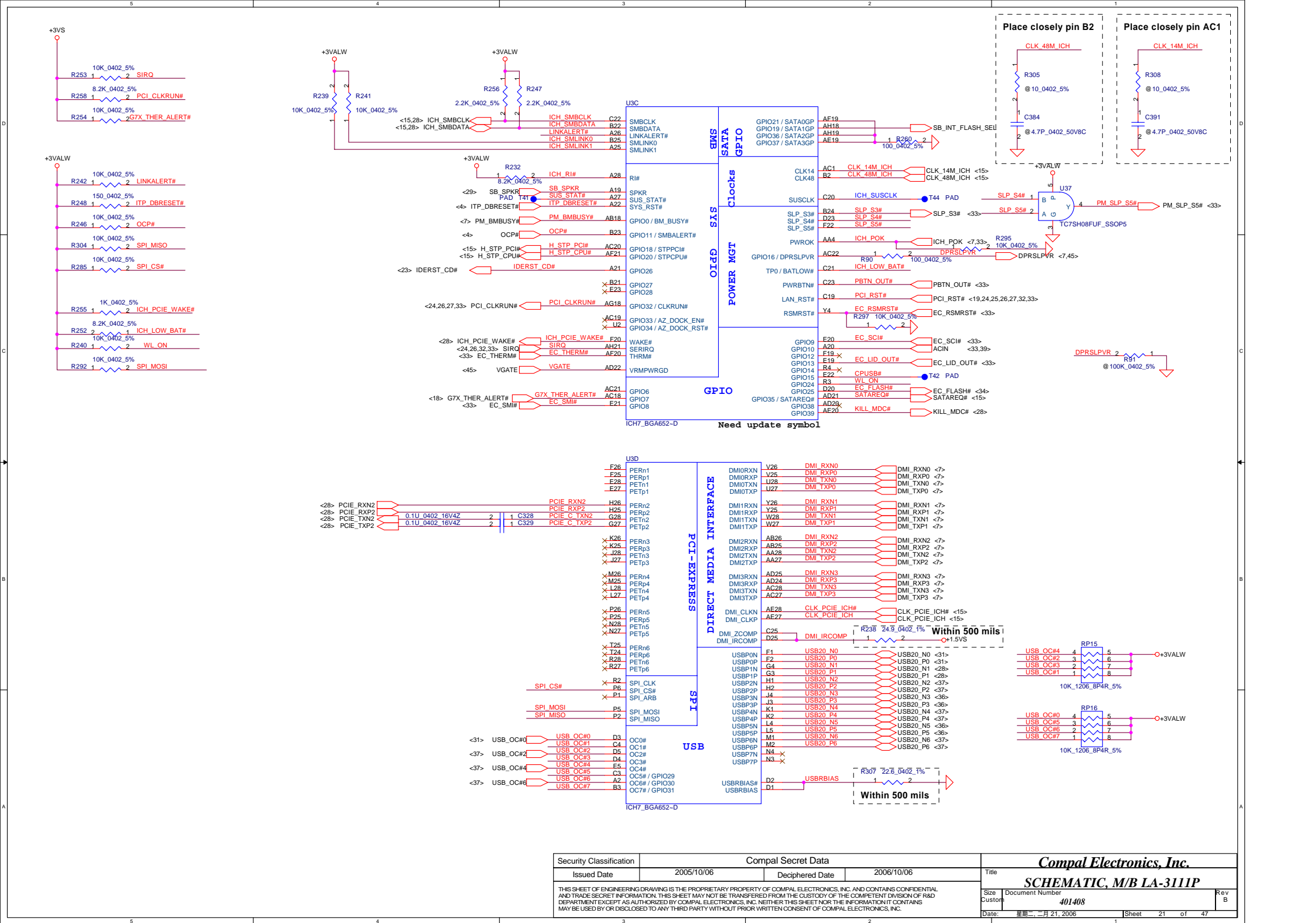
Place closely pin A9

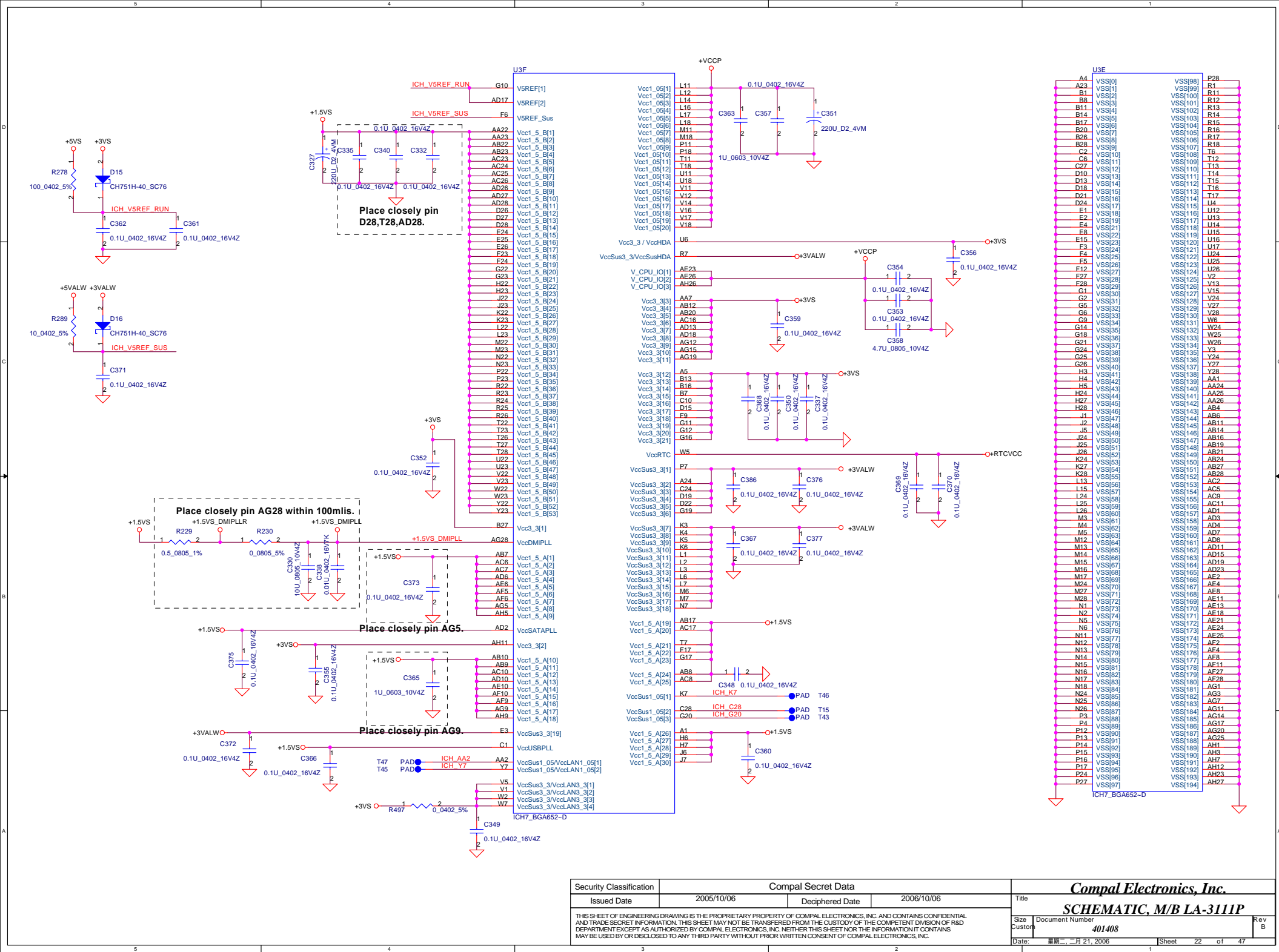


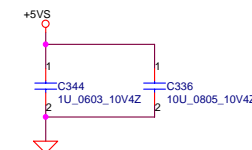
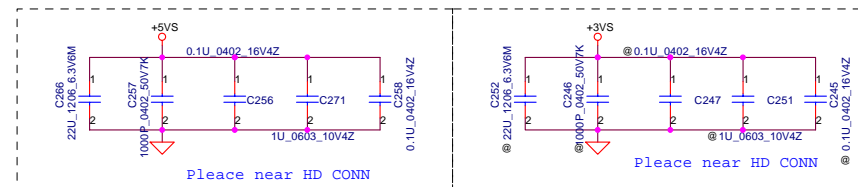
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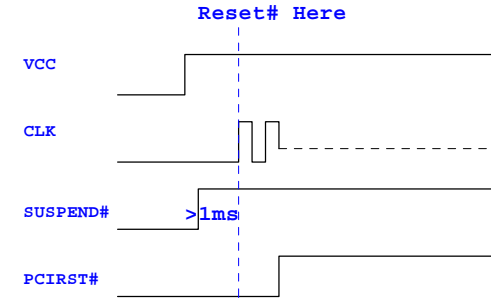




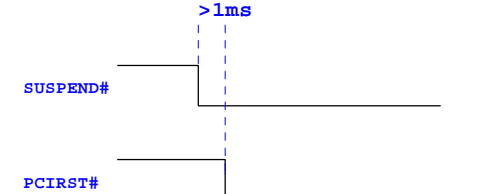


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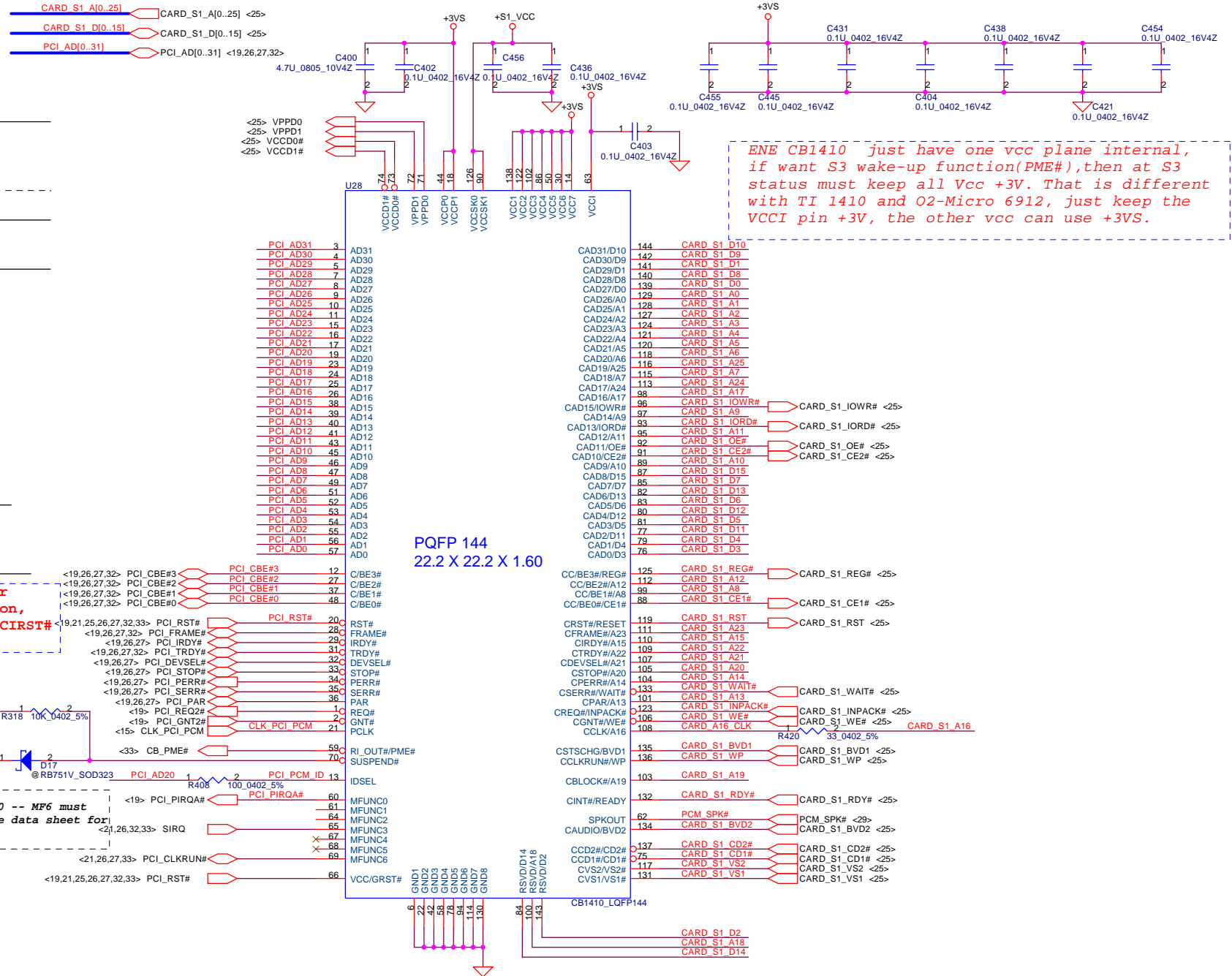
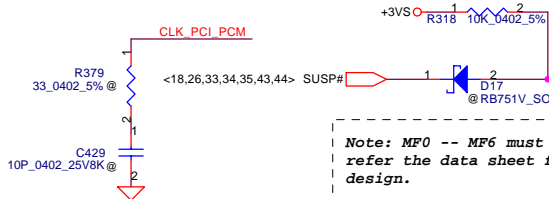
Power on RESET#



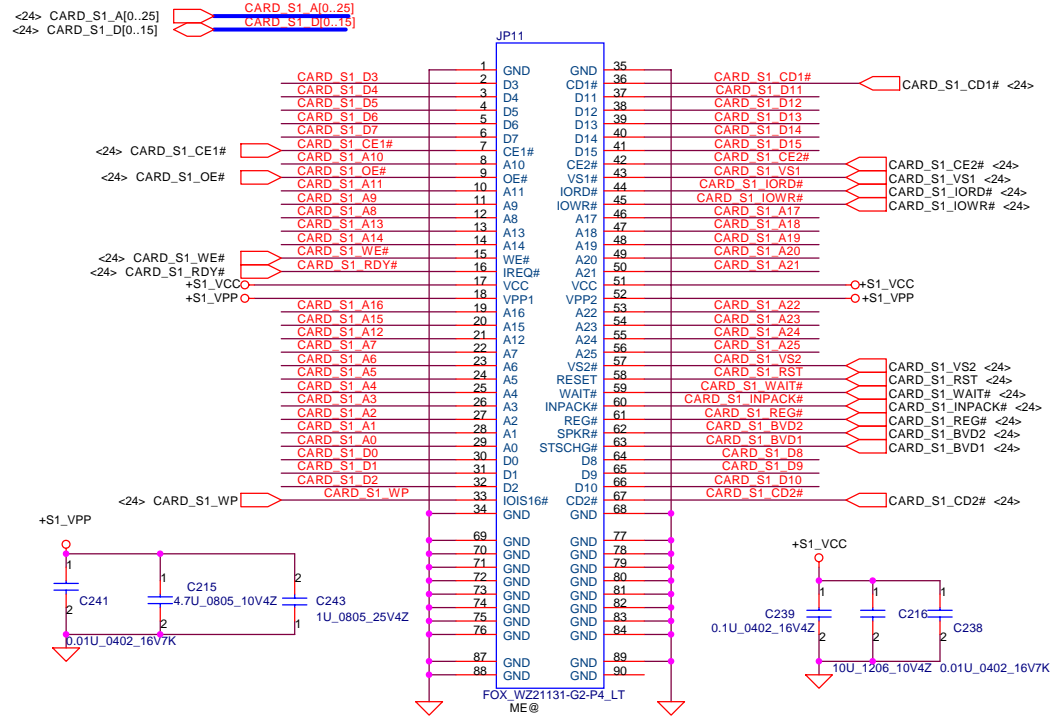
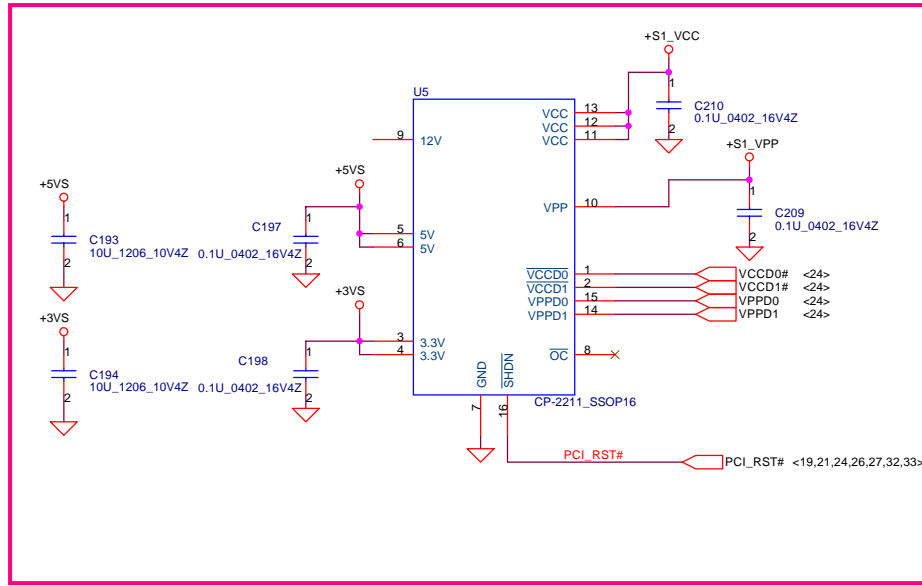
Entry S3



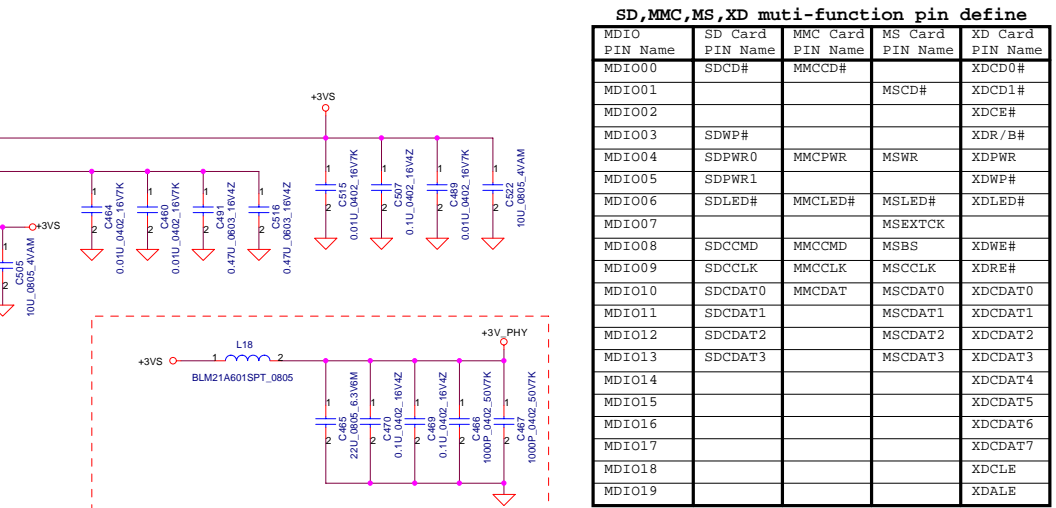
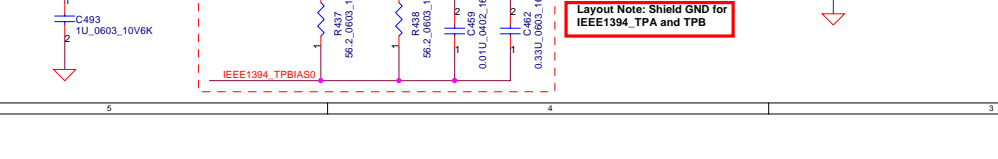
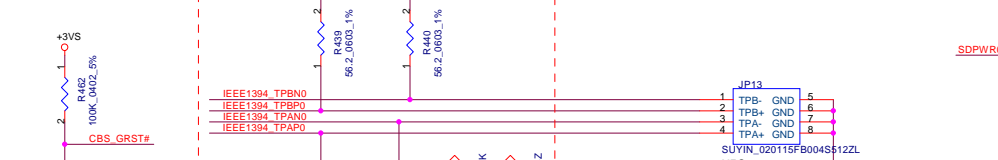
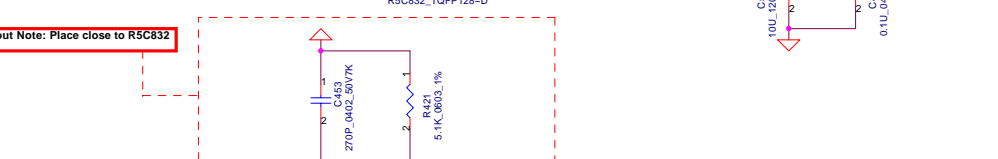
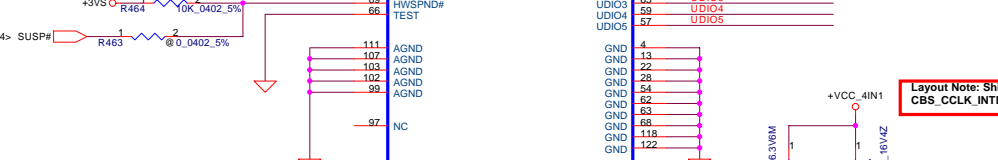
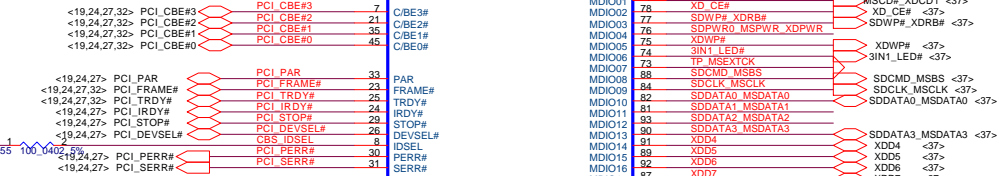
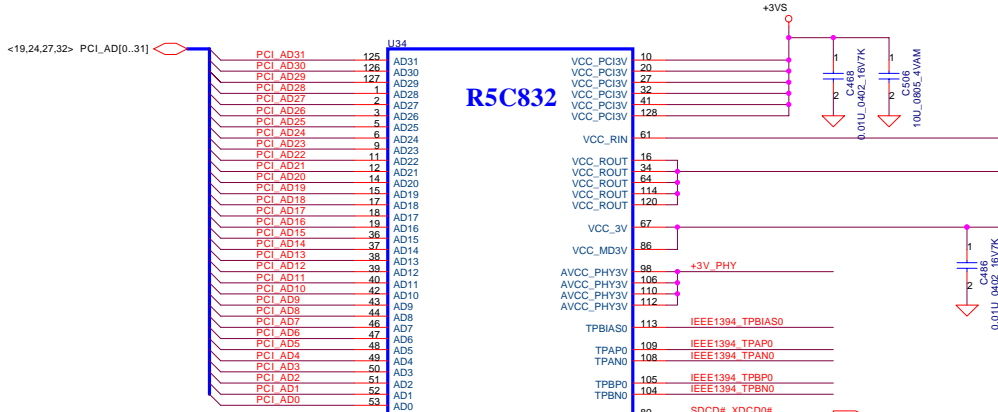
SUSPEND# will gate the PCIRST# or GRST#, so need S3 wake up function, SUSPEND# must be LOW ahead the PCIRST# about 1ms.



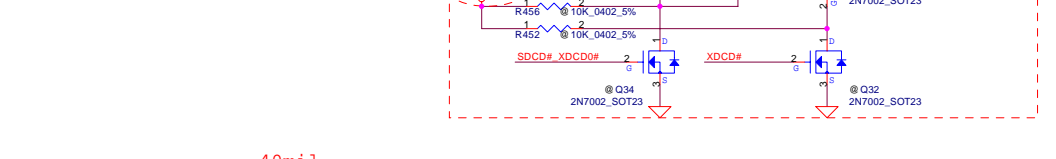
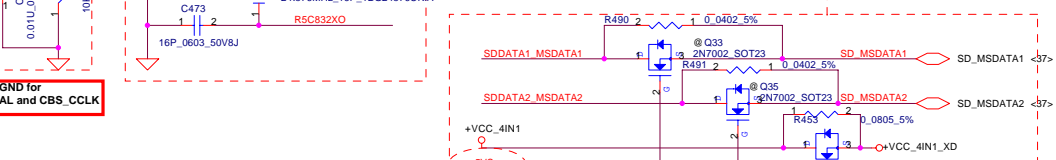
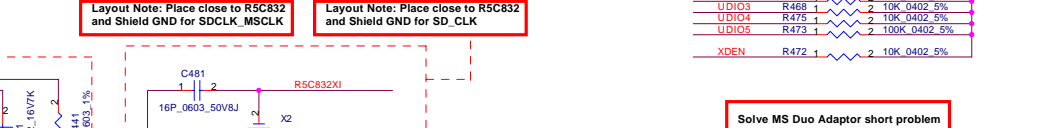
PCMCIA Power Controller



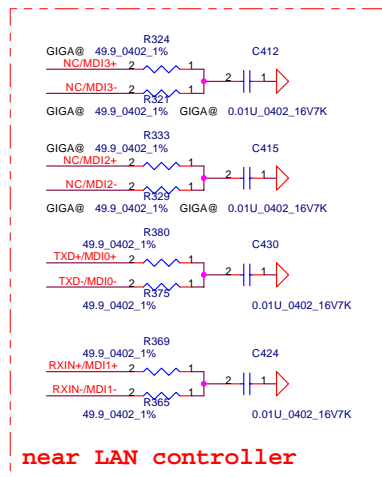
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Function set pin define				
UDIO03	UDIO04	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-up	Enable SD, XD, MS, MMC Card

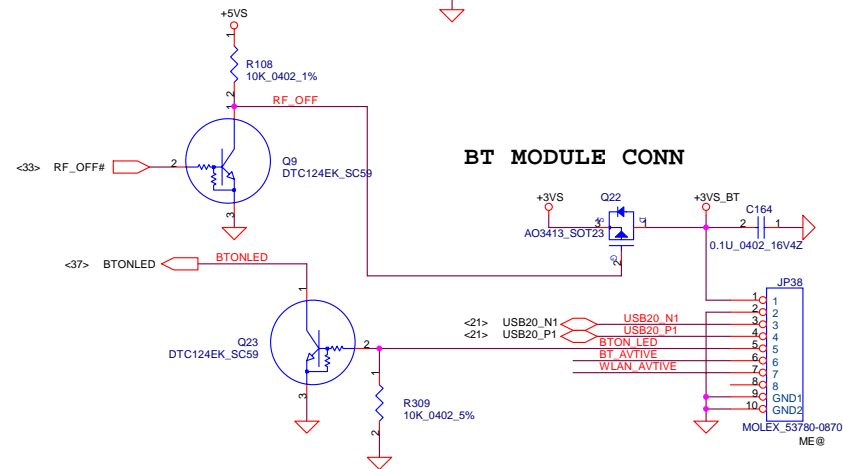
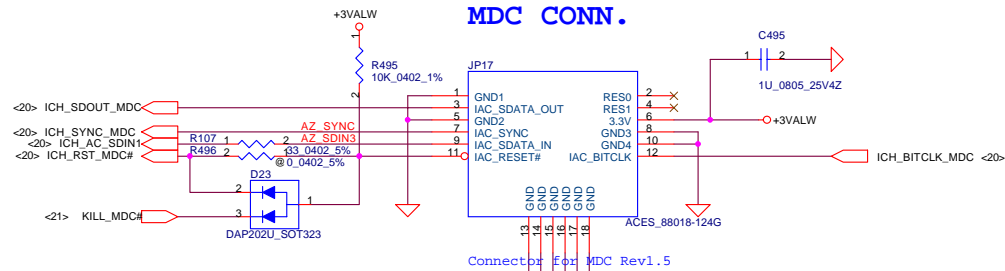
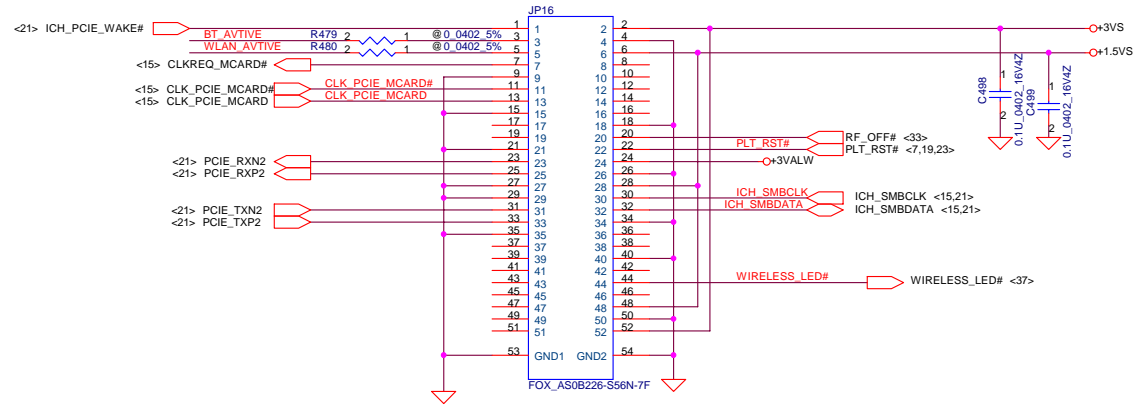


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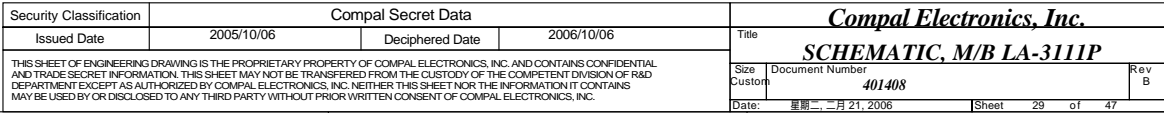


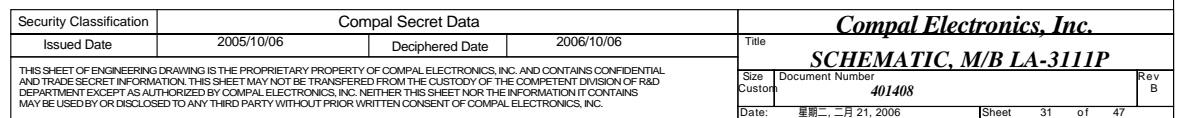
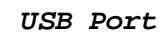
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Mini-Express Card(Slot 1-WLAN)

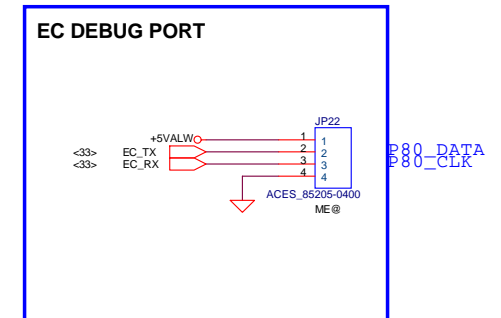
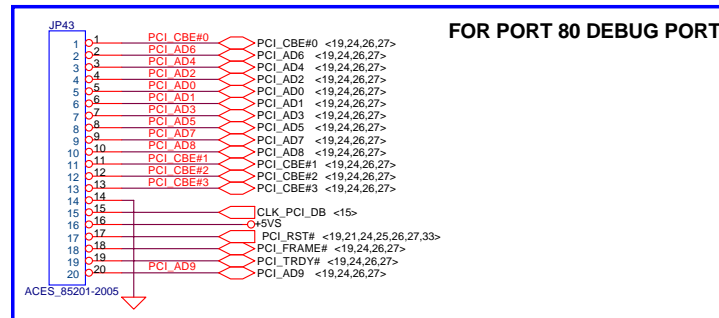
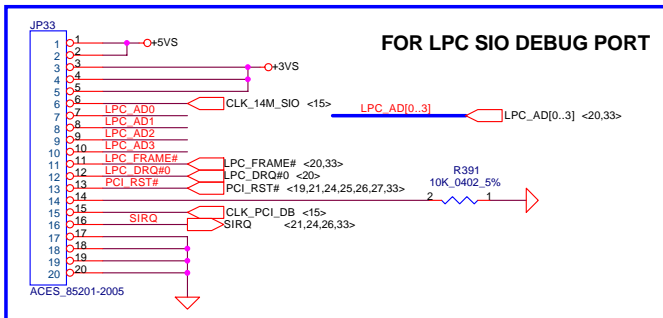
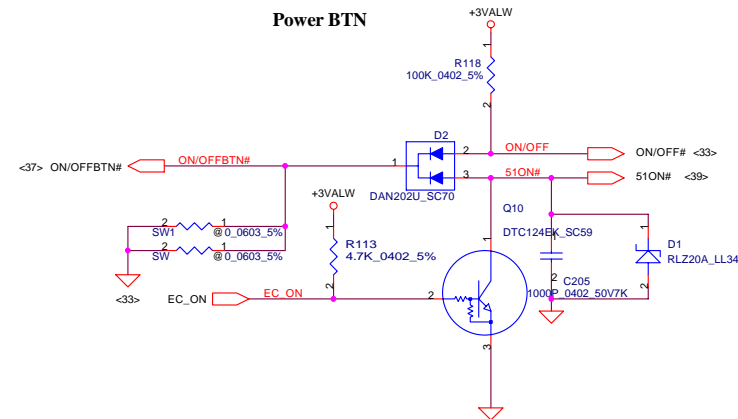
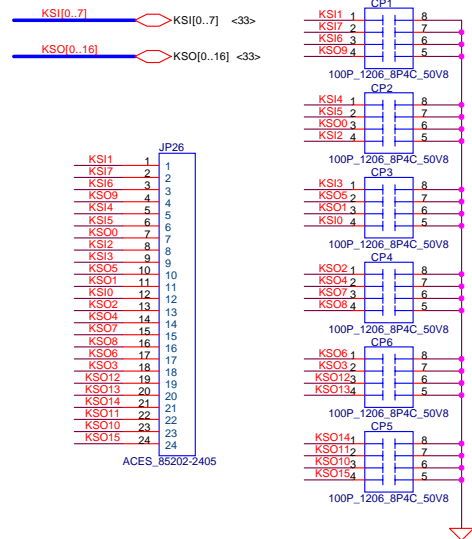


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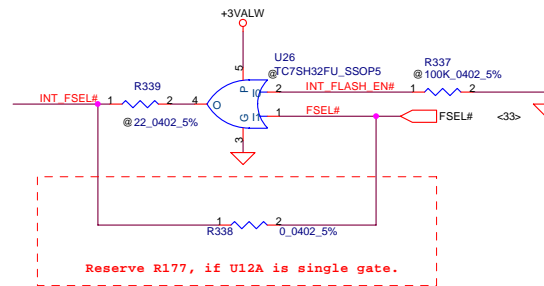
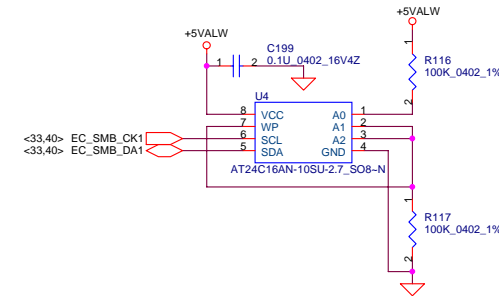
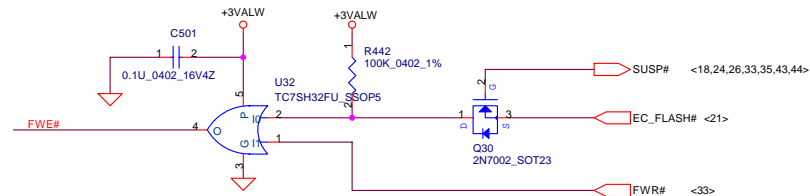




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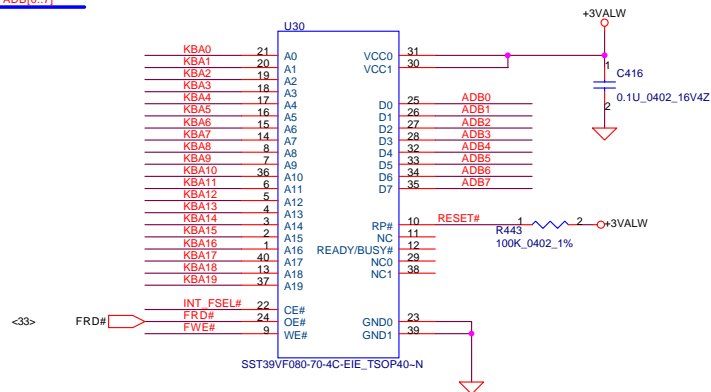


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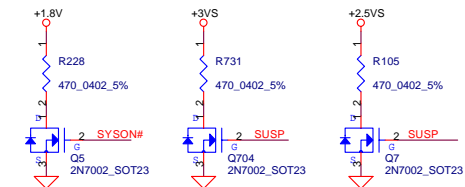
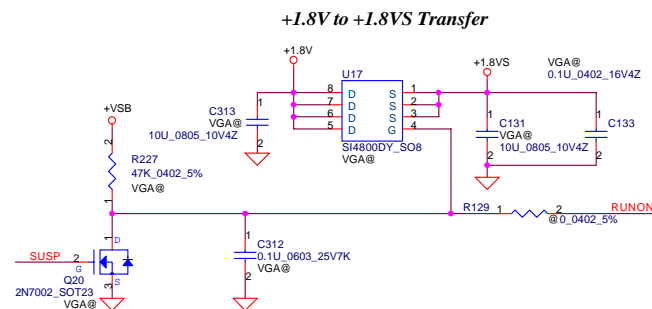
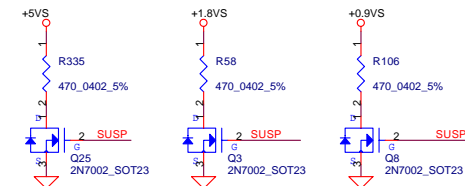
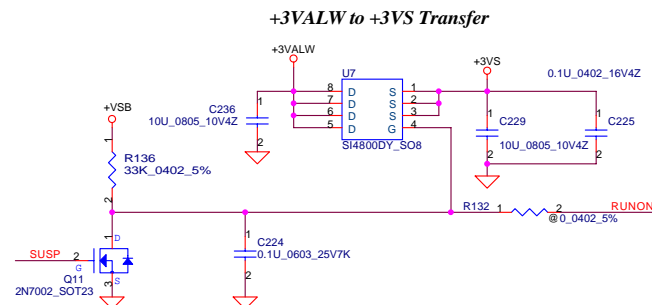
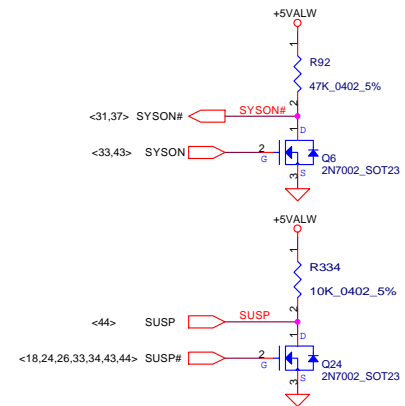
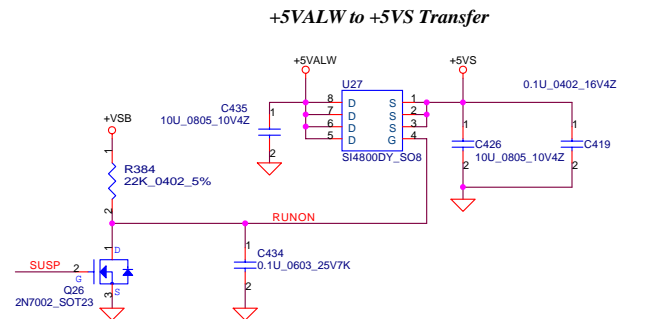


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<33> ADB[0..7] ADB[0..7]

1MB Flash ROM

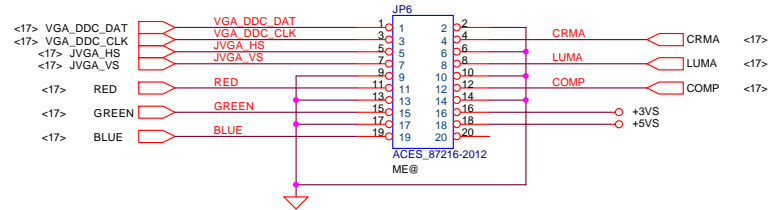


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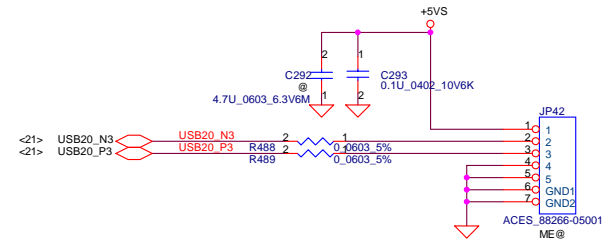


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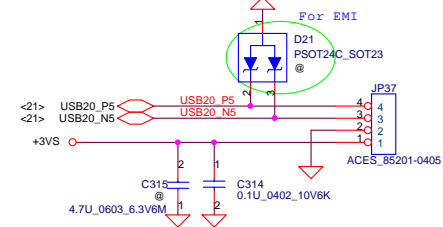
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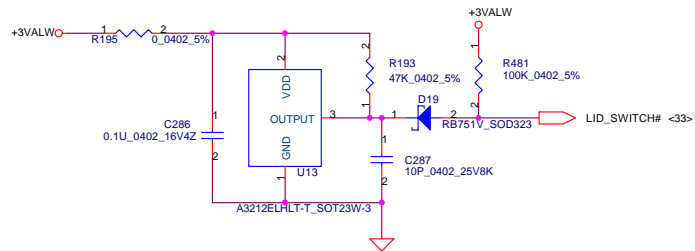
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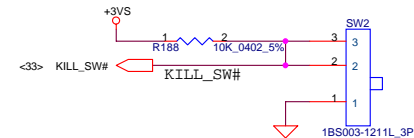
Finger Print board



LID Switch

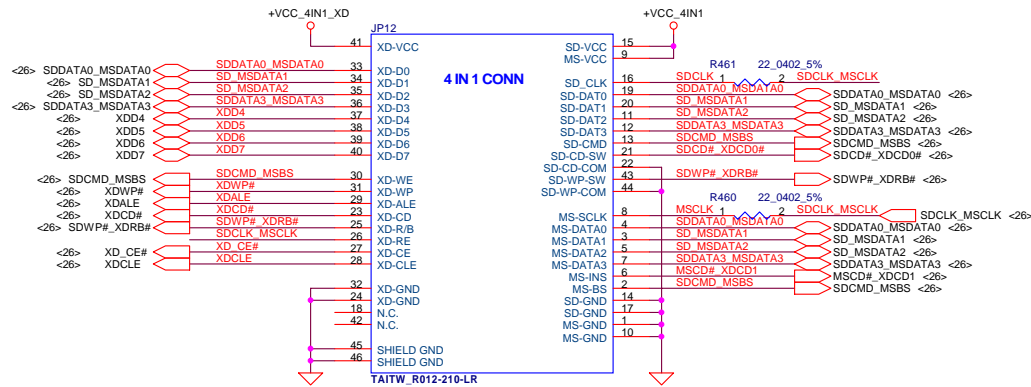


Kill Switch

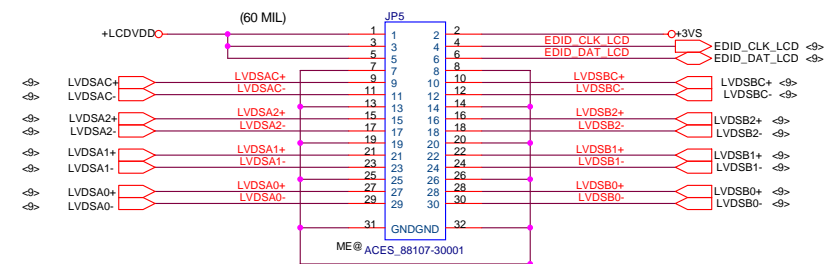


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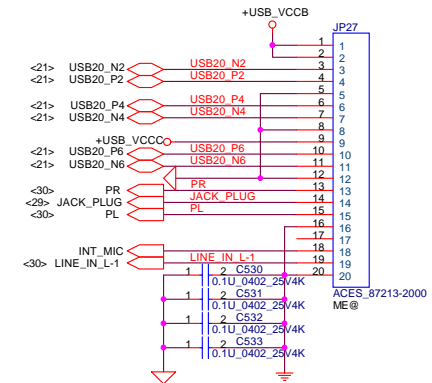
4 in 1 Card Reader



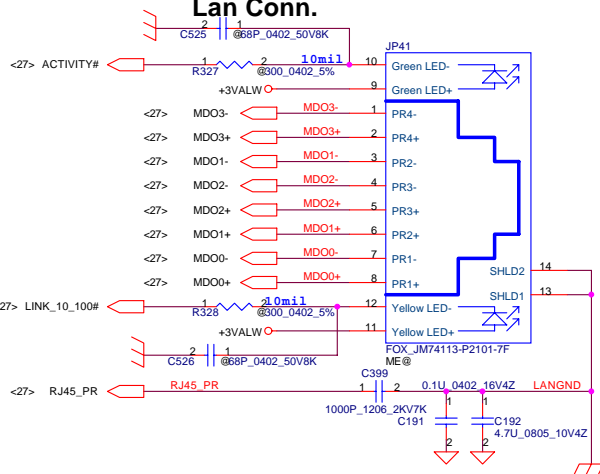
UMA LCD/PANEL Conn.



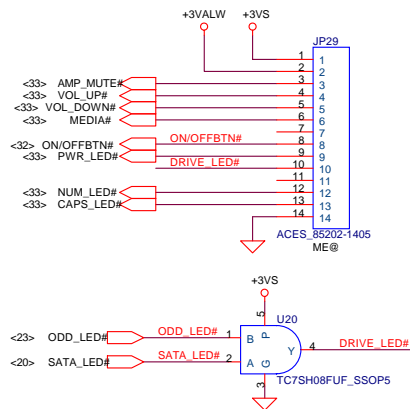
Audio Jack/USB Conn.



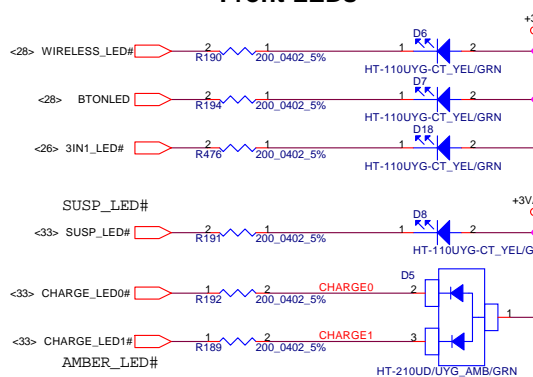
Lan Conn.



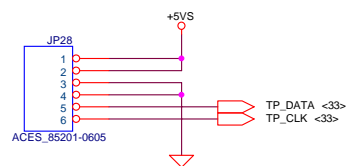
PWR ON/OFF SW & LED



Front LEDs



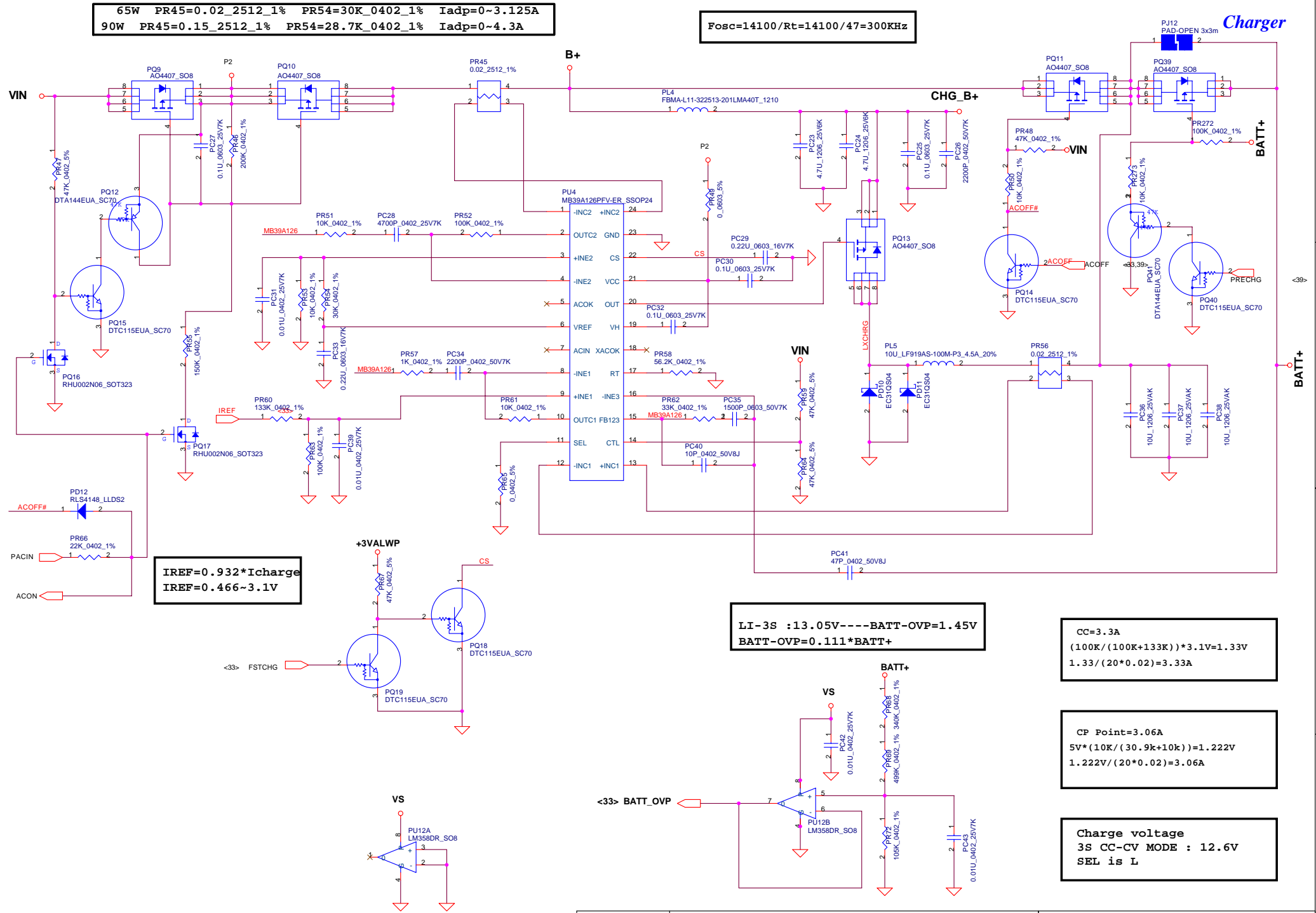
T/P Board



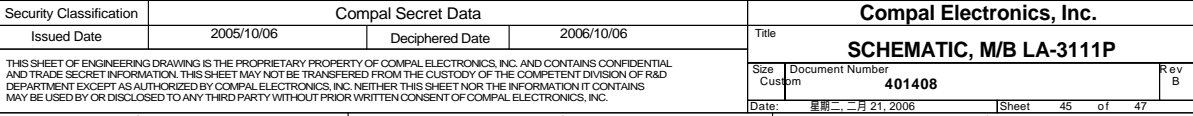
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Item	Fixed Issue/Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
B Test						
1	Implement S4	0.2	21	Add U37(TC7SH08FUF) 1. Connect U37 pin1(SLP_S4#) ,pin2(SLP_S5#) to U3(SB) 2. Connect U37 pin4(PM_SLP_S5#) to U6(EC) pin17 3. Del R482"		
2	Change ICH7M GPIO pin control	0.2	21	Change G7X_THER_ALERT# net from U3 (ICH7M) pin AD20 (GPIO 38) to pinAC18 (GPIO7)		
3	SD/XD card can't work/Reverse solve MS Duo short solution	0.2	26	Add a D22(DAN202U),R490,R491 1. Connect D22 pin3 to MSCD#_XDCD0 2. Connect D22 pin2 to MSCD#_XDCD1 3. Connect D22 pin1 to JP12 pin23(XDCD#) 4. Connect R490 pin2 to SDDATA1_MSDATA1 5. Connect R490 pin1 to SD_MSDATA1 6. Connect R491 pin2 to SDDATA2_MSDATA2 7. Connect R491 pin1 to SD_MSDATA2 Change R456,Q33,Q35 to no stuff		
4	Set amplifier gain	0.2	30	Connect U36 pin 7 to R486 pin 2		
5	Add ADP_ID	0.2	33	1. Connect R401 pin1 to PR213 pin2		
6	Support wake on Ring/Disable MDC function	0.2	28	1. Change JP17 pin6 from +3VS to +3VALW 2. Add R495,D23 3. Connect D23 pin1/2 to ICH_RST_MDC# 4. Connect D23 pin3 to ICH7M GPIO		
7	HD Audio design change	0.2	29	1. Change line out from pin 35/36 to pin 43/45 2. Add R494 and connect R494 pin 1 to R166 pin 2 3. Connect R494 pin 2 to +AVDD_AC97 4. Add C527/C528/C529/C530 for EMI		
8	VCCLAN3_3 power plant change	0.2	22	Connect U3(ICH7M) pin V5/V1/W2/W7 to +3VS		
9	Reverse +3VS for Lan power	0.2	27	1. Add R498,R499 2. Connect R498 pin1 to +3VS and Connect R499 pin 1 to +3VALW 3. Connect R498/R499 pin 2 to +3V_LAN		
10	Finger print connector change	0.2	27	Change JP37 from ACES_85201-0605 to ACES_85201-0405		
11	Change KB910L GPIO pin control	0.2	33	Change SUSP_LED# from U3 (KB910L) pin 35 to pin 102		
C Test						
12	EMI solution	0.3	31/37	Add C531,C532,C533,C534,C535		
13	Solve HP bo issue	0.3	30	1. Add Q701,Q702,R727,R728 2. Add Q703,R729 to change EAPD phase 3. Connect EAPD# to R727,R728		
14	Solve Speaker bo issue solution	0.3	30	1. Connect EAPD to EC pin 94 2. Change EC_Mute sequence to solve this issue		

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